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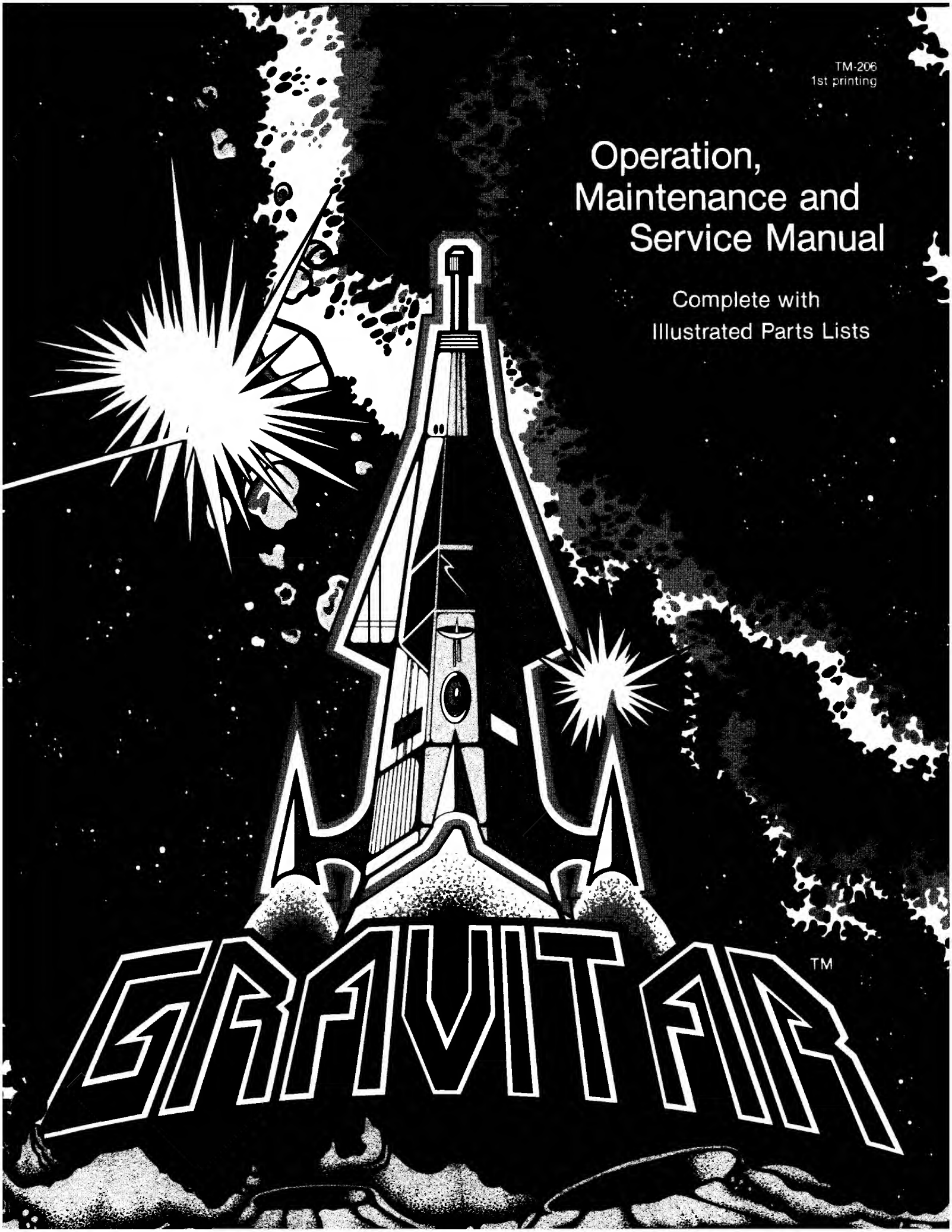
1st printing

Operation, Maintenance and Service Manual

Complete with
Illustrated Parts Lists



Operation, Maintenance and Service Manual

Complete with Illustrated Parts Lists

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Lithographed in the U.S.A. **7L**

Notice Regarding Non-ATARI Parts

WARNING

Use of non-ATARI parts or modifications of your ATARI game circuitry may adversely affect the safety of your game, and may cause injury to you and your players.

The warranty printed on the inside back cover of this manual may be voided, if you do any of the following:

- Substitute non-ATARI parts in your coin-operated game, or
- Modify or alter any circuits in your ATARI game by using kits or parts *not* supplied by Atari.

The use of any non-ATARI parts will void the warranty, and any such alteration may also adversely affect the safety of the game and may cause injury to you and your players.

to licensed communications services is not permitted by the FCC (Federal Communications Commission).

If you suspect interference from an ATARI game at your location, check the following:

- All grounds (green wires) in the game are properly connected as shown in the game wiring diagram, and
- The power cord is properly plugged into a *grounded* 3-wire outlet.

If you are unable to solve the interference problem, please contact ATARI Customer Service. See page vi for service in your area.

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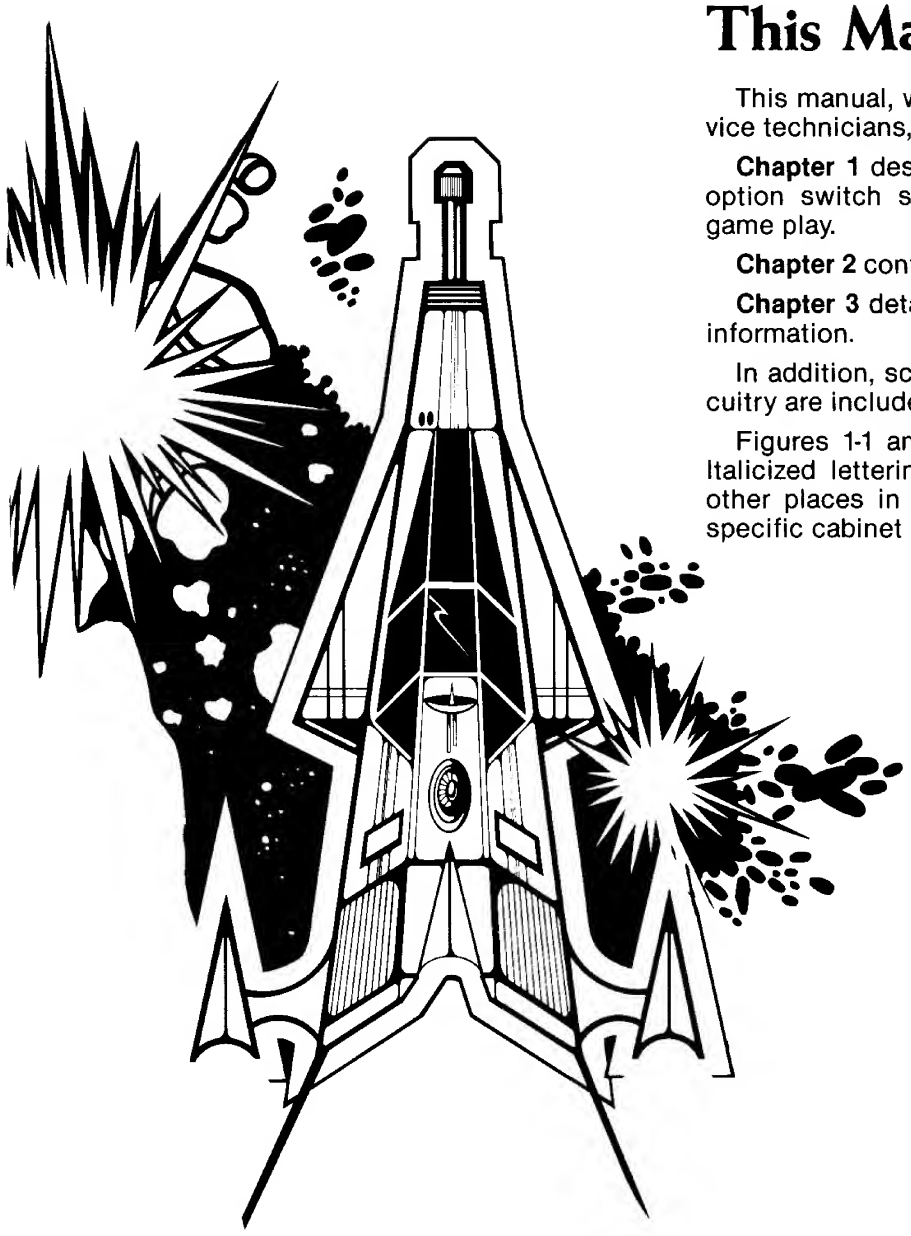
Set-Up Procedures



How to Use This Manual

This manual, written for game operators and service technicians, describes the Gravitar™ game.

Chapter 1 describes new features, game setup, option switch settings, self-test procedures, and game play.

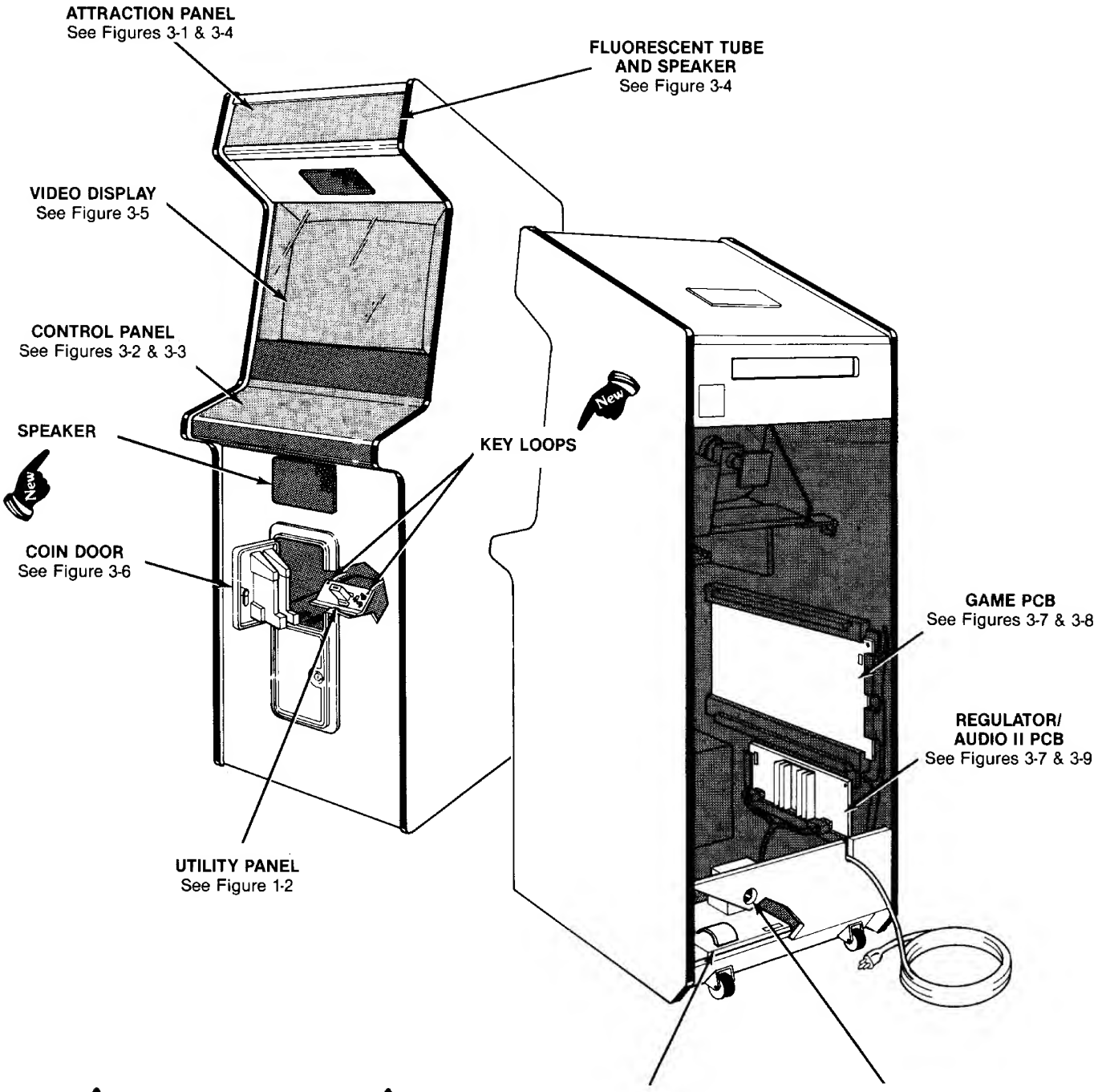
Chapter 2 contains troubleshooting procedures.

Chapter 3 details maintenance, repair, and parts information.

In addition, schematic diagrams of the game circuitry are included with this manual.

Figures 1-1 and 3-1 illustrate the game cabinet. Italicized lettering on these figures refers you to other places in the manual for information about specific cabinet parts.

Chapter 1



WARNING
SHOCK HAZARD

Connect this game only to a grounded 3-wire outlet. If you have only a 2-wire outlet, we recommend you hire a licensed electrician to install a grounded outlet. *Players may receive an electric shock* if this game is not properly grounded!

Figure 1-1 Game Overview

A. New Features

The Gravitar™ game has four new features. Even if you are familiar with ATARI® games, you should note these important differences:

1. **Shielded Game Speakers.** These 8-ohm, 6-ounce, high-fidelity speakers provide exceptional audio. The speaker magnets are shielded.
2. **Key Loops.** The utility panel has two key loops. They provide a convenient place to store keys for the rear access panel and lower coin door.
3. **High-Score Table.** There are eight different titles for the high-score table. The title is determined by the highest score registered (see *G. Game Play*).
4. **Molded Coin Box.** This game has a sleek, one-piece molded coin box with handles on either end for easier carrying.

New features and all other major parts in the game are illustrated in Figure 1-1. Throughout this manual, wherever one of these new features is mentioned, you will see this symbol:

B. Game Inspection

Please inspect your game carefully to ensure that it was delivered to you in good condition.

NOTE

Do not plug in the game yet!

1. Examine the exterior of the game cabinet for dents, chips, or broken parts.
2. Remove the screws that were used as extra security to seal the rear access panel. Unlock and open this panel and the coin door; inspect the interior of the game as follows:
   a. Ensure that all plug-in connectors (on the game harness) are firmly plugged in. Replug any connectors found unplugged. **Don't force connectors together.** The connectors are keyed so they only fit in the proper orientation. **A reversed edge connector may damage a PCB** and will void your warranty.
   b. Ensure that all plug-in integrated circuits on the PCB are firmly plugged into their sockets.
   c. Remove the tie-wrap that secures the coiled power cord inside the cabinet. Inspect the power cord for any cuts or dents in the insulation. Repair or replace it as required. Place the square black plastic strain-relief plate in the wood slot at the bottom of the rear panel opening.

WARNING

To avoid electrical shock, do not touch internal parts of the display with your hands or with metal objects held in your hands!

   d. Note the game serial number. It is printed on a label on the back of the cabinet. Verify that the same serial number is also on the Gravitar game PCB, Regulator/Audio II PCB, power supply, and video display. A drawing of the serial-numbered components is on the inside front cover of this manual. Please mention this number whenever you call your distributor for service.
   e. Inspect major subassemblies, such as the power supply, control panel, and video display, for secure mounting.

C. Game Installation

1. Installation Requirements

Power	200 W
Temperature	0 to 38°C (32 to 100°F)
Humidity	Not over 95% relative
Space Required	64 x 80 cm (25 ½ x 31 ½ in.)
Game Height	184 cm (72 ½ in.)

2. Voltage Selection

The power supply used in this game operates on the line voltage of almost any country in the world. The power supply comes with either one, two, or three different voltage selection plugs. Plug voltages and wire colors are 100 VAC (violet wire color), 120 VAC (yellow wire color), 220 VAC (blue wire color), and 240 VAC (brown wire color).

Before plugging in your game, check your line voltage. Then check the wire color on the voltage selection plug that is plugged into your power supply. Make sure the voltage selection plug is correct for your location's line voltage (see *Figure 3-10*).

D. Switch Locations

1. On/Off Switch

The on/off switch is located on the back of the cabinet, lower left side (see *Figure 1-2).*

2. Utility Panel Switches

The utility panel includes the volume control, self-test switch, coin switch, and coin counter(s). The coin switch is used to credit the game, and it activates the left coin counter. These switches are located inside the upper coin door (see *Figure 1-2).*

3. Option Switches

Option switches are located on the game PCB (see *Figure 1-2).*

a. Game price options are at PCB location B4.
b. Game play options are at PCB location D4.
c. Special options are at PCB location P10/11.

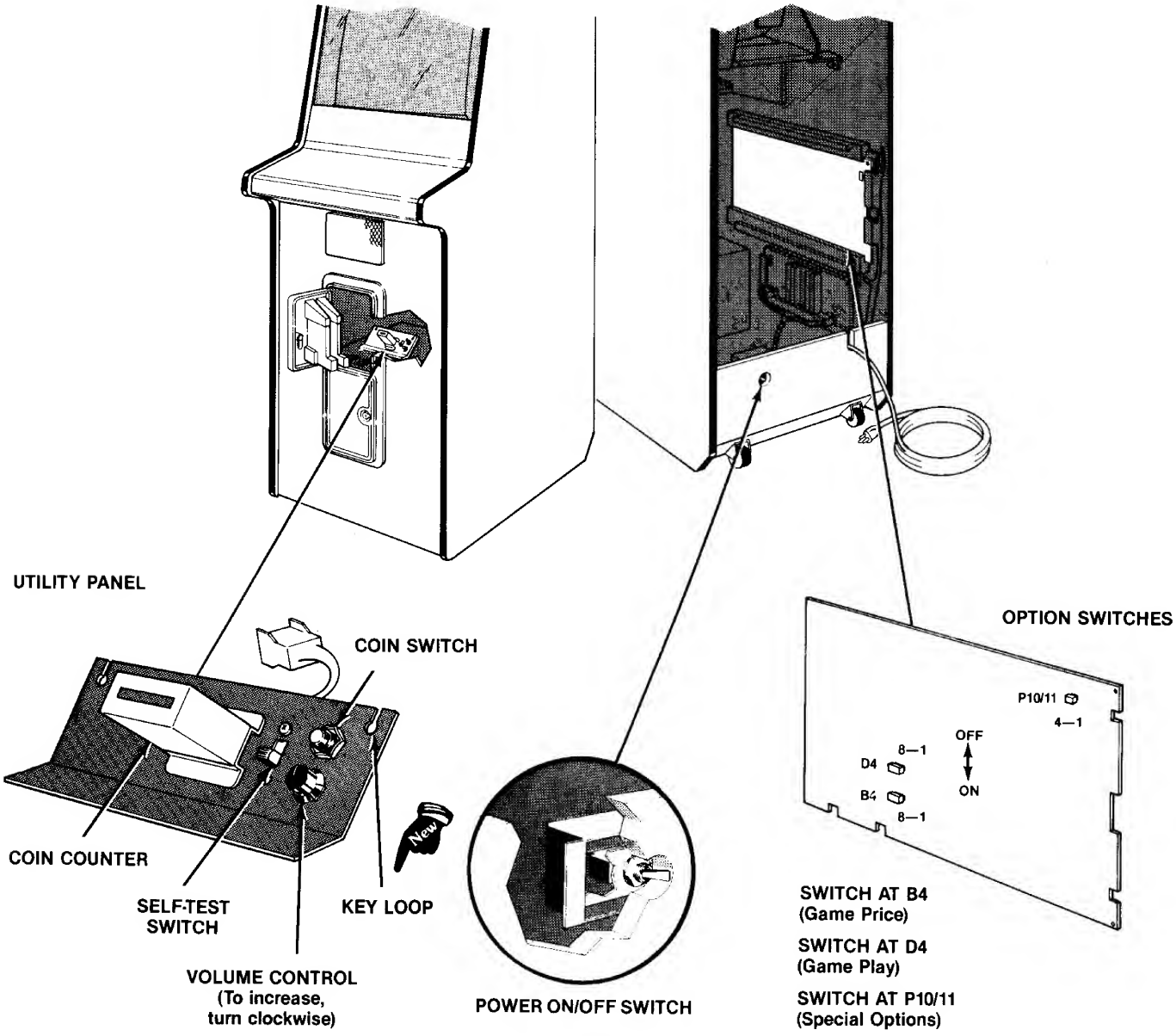


Figure 1-2 Game Switch Locations

E. Option Switch Settings

Tables 1-1, 1-2, and 1-3 detail game option switch settings. Options are preset at the factory and shown by the ◄ symbols. However, you may change the settings to suit your individual needs.

To verify option switch settings, power the game *off* and then *on* again. Set the self-test switch to *on* and verify the settings on the self-test screen. Then set the self-test switch to *off.*

Table 1-1 Game Price Options

This table contains the switch settings for options relating to game price, coin mechanism multipliers, and bonus play. The switches are on the game PCB at location B4 and are accessible when the game PCB is mounted in place.

The *coin mechanism* is a device on the inside of the coin door that inspects the coin to determine if the correct coin has been inserted. After this inspection, the mechanism either accepts or rejects the coin.

The *multipliers* (toggles 4-6) determine how much each coin mechanism will be worth to the game's logic. The coin door has two mechanisms.

The basic unit of measurement is a coin worth $.25 or 1 DM, which equals a multiplier of x1. Therefore, if you have a 2 DM/1 DM coin door, you may want to set the left multiplier at x2 and the right multiplier at x1.

You may offer *bonus play* for certain combinations of coins inserted. For example, with the game set at $.25 per play, players who deposit four successive quarters, then press the start switch, can receive a bonus play. The bonus feature encourages players to insert more money than just the minimum $.25 required for one game. All coins must be inserted before pressing the start switch.

Settings of 8-Toggle Switch on Gravitar PCB *(at B4)*								Option
8	7	6	5	4	3	2	1	
Off	On							Free play
On	On							1 coin for 2 credits
Off	Off							1 coin for 1 credit ◄
On	Off							2 coins for 1 credit
		Off	Off					Right coin mechanism x 1 ◄
		On	Off					Right coin mechanism x 4
		Off	On					Right coin mechanism x 5
		On	On					Right coin mechanism x 6
				Off				Left coin mechanism x 1 ◄
				On				Left coin mechanism x 2
					Off	Off	Off	No bonus coins ◄
					Off	On	Off	For every 4 coins inserted, logic adds 1 more coin
					On	On	Off	For every 4 coins inserted, logic adds 2 more coins
					Off	Off	On	For every 5 coins inserted, logic adds 1 more coin
					On	Off	On	For every 3 coins inserted, logic adds 1 more coin
					Off	On	On	No bonus coins
					On	On	On	No bonus coins

◄ *Manufacturer's recommended settings*

Table 1-2 Special Options

Settings of 4-Toggle Switch on Gravitar PCB *(at P10/11)*				Option
4	3	2	1	
			On	Credits counted on one coin counter.
			Off	Credits counted on two separate coin counters

Table 1-3 Game Play Options

This table contains the switch settings for options relating to game difficulty, language, bonus, and ships. The switches are on the game PCB at location D4, and are accessible when the game PCB is mounted in place.

Settings of 8-Toggle Switch on Gravitar game PCB *(at D4)*								Option
8	7	6	5	4	3	2	1	
						On	On	No bonus
						Off	Off	Bonus ship every 10,000 points ◄
						On	Off	Bonus ship every 20,000 points
						Off	On	Bonus ship every 30,000 points
Not used	*Not used*				*Not used*			
				On				Easy game play ◄
				Off				Hard game play
		Off	Off					3 ships per game
		On	Off					4 ships per game ◄
		Off	On					5 ships per game
		On	On					6 ships per game

◄*Manufacturer's recommended settings*

F. Self-Test Procedure

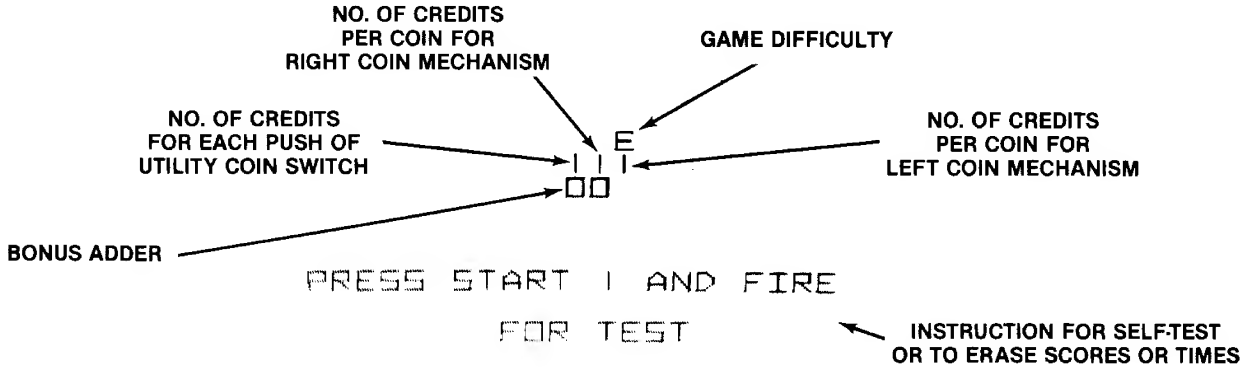
This game will test itself and provide data to show that the game's circuitry and controls are operating properly. The data is provided on the video display and speaker. No additional equipment is necessary.

We suggest you perform the self-test procedure when you first set up the game, any time you collect money from the game, when you change game options, or when you suspect game failure.

Wait at least 10 seconds after playing a game before entering self-test. Otherwise you may erase the top three scores in the high-score table or distort the statistics. All credits will be cancelled when you enter self-test.

Refer to *Figure 1-2* for the location of the self-test switch and option switches. To see the Operator Information Display, set the self-test switch to *on* (see *Figure 1-3*). To enter self-test, hold the FIRE button down while pressing 1-player start (see *Figure 1-4*). To end the self-test, set the self-test switch to *off*.

The complete self-test procedure is explained in *Chapter 2, Self-Test Procedure*. If a part of the test described in Figure 1-4 fails, refer to Chapter 2.



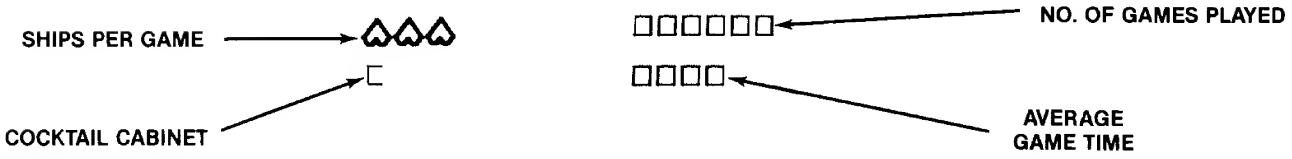


Figure 1-3 Operator Information Display

The Operator Information Display shows game statistics. You may also erase game scores and times. To see this display, set the self-test switch to *on*.

To erase game scores:
1. Push 1-PLAYER START until display reads *PRESS START 1 AND FIRE TO CLEAR SCORES.*
2. Press both FIRE and 1-PLAYER START.
3. The word *ERASING* flashes on the screen until the entire table is erased. **Wait** until the word *ERASING* disappears before going on with other tests.

To erase game times:
1. Push 1-PLAYER START until display reads *PRESS START 1 AND FIRE TO CLEAR TIMES.*
2. Press both FIRE and 1-PLAYER START.
3. The word *ERASING* flashes on the screen until the entire table is erased. **Wait** until the word *ERASING* disappears before going on with other tests.

To erase game scores and times:
1. Push 1-PLAYER START until display reads *PRESS START 1 AND FIRE TO CLEAR TIMES AND SCORES.*
2. Press both FIRE and 1-PLAYER START.
3. The word *ERASING* flashes on the screen until the entire table is erased. **Wait** until the word *ERASING* disappears before going on with other tests.

To end the Operator Information Display, set the self-test switch to *off*.

Table 1-4 Self-Test Procedure

	Instruction	Test Passes
1.	Set the self-test switch to *on.* While holding the FIRE button down, press 1-player start.*	The screen shows the self-test display. RAMs, ROMs, and three integrated circuits are tested. If the screen is different from the self-test display, or if there are sounds, refer to *Chapter 2, Self-Test Procedure.*
2.	Activate control panel and coin switches.	As you activate the switches, you should hear a beep and the proper *0* should change to *1.* If the test fails, refer to *Chapter 2, Self-Test Procedure.*
3.	Observe the white frame at the sides of the screen.	Each frame corner should be within ¼-inch of each display bezel corner. If the test fails, refer to *Chapter 2, Self-Test Procedure, Screen 2.*

**All credits are cancelled when you enter self-test*

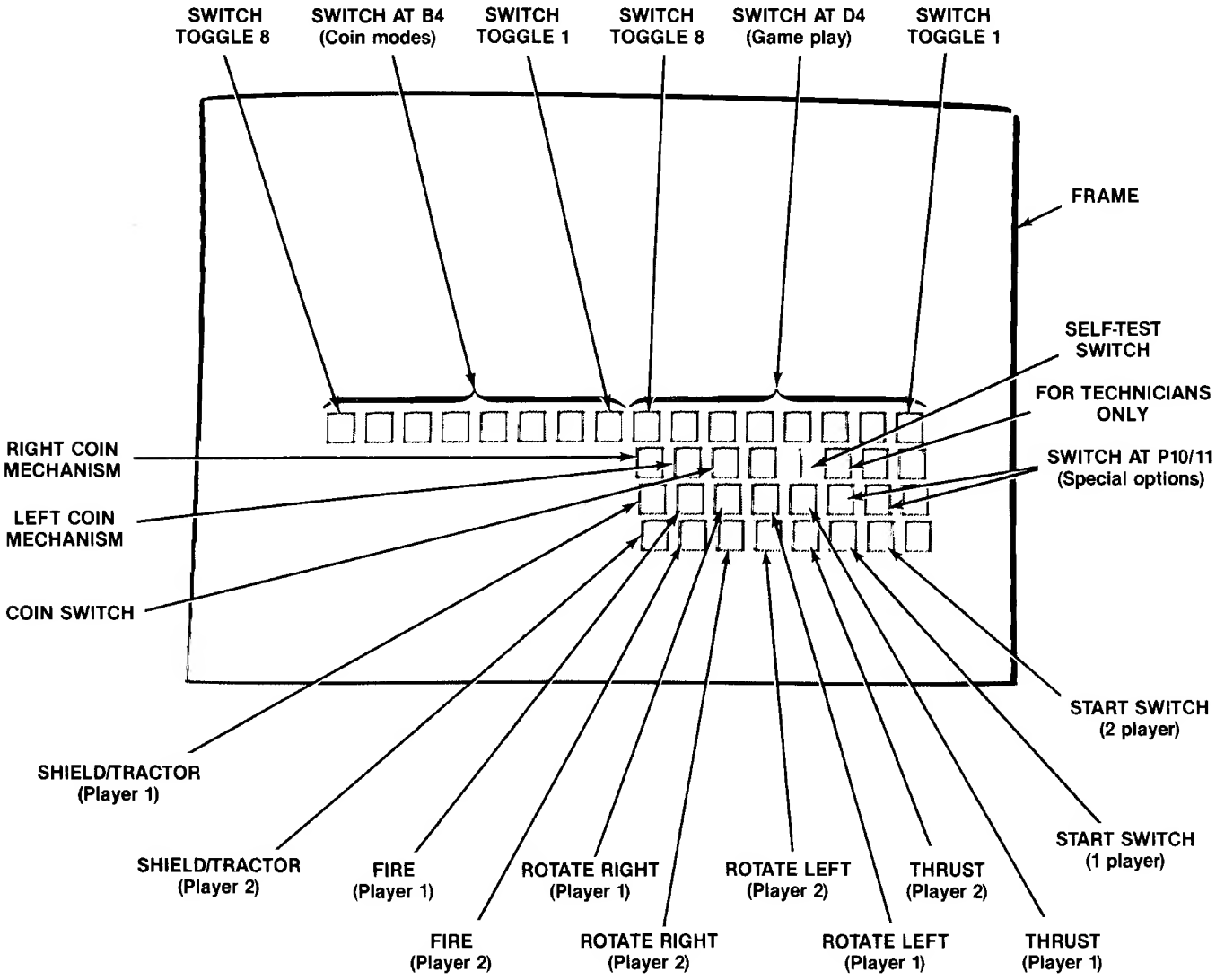


Figure 1-4 Self-Test Display

G. Game Play

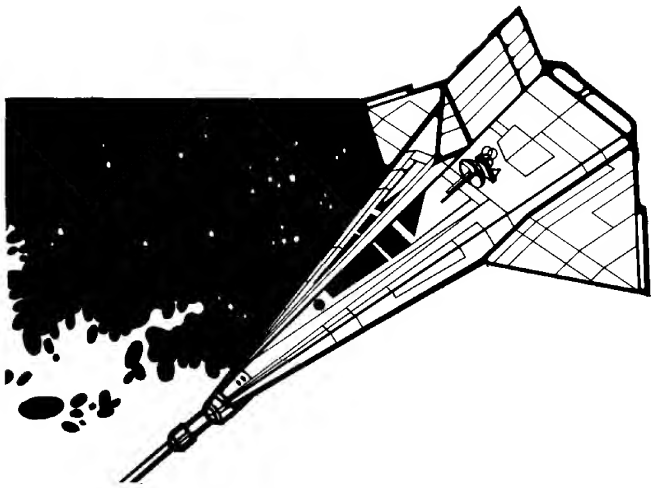
Gravitar™ is a one- or two-player game with a color X-Y video display. This new display, with its 3 color guns and higher voltage, has the same technology that was used in previous Atari black-and-white X-Y displays. However, the screen now displays dazzling colors and unique visual effects.

The player controls a space ship in three different solar systems. Each solar system consists of a home base, a death star, a red alien planet and four regular planets. Each planet has its own unique terrain.

The red alien planet is the home of shooting alien ships. Some of the regular planets may have flying alien rammers to be avoided or shot down. The four planets all have fuel cells to be retrieved with a tractor beam and alien bunkers that fire shells. Successfully destroying all of the bunkers results in a MISSION COMPLETE message at the top of the screen. Achieving MISSION COMPLETE allows the player to collect bonus if he can evade the rammers when leaving the planet. If successful, he will be placed back in the solar system.

A player has two ways to advance to the next solar system. The first is to successfully complete a mission on all four regular planets. The second way is to complete a mission on the red alien planet, which establishes a link into the next solar system.

Gravitar™ has five possible modes of operation: demonstration, attract, play, high-score, and self-test. Self-test is a special mode for checking the game switches and computer functions. You may enter self-test at any time. Wait at least ten seconds after a game has been played before entering self-test or turning off power; otherwise, you may erase the high-score table.



1. Demonstration Mode

The demonstration mode allows the operator to enter all planets to see their respective terrains and obstacles without being destroyed by shots from bunkers or alien space ships, or being hit by flying alien rammers. Enter this mode when you are in the *Operator Information Display* (see *Figure 1-3*) by simultaneously pressing all five player control buttons. To end this mode, set the self-test switch to *off.*

2. Attract Mode

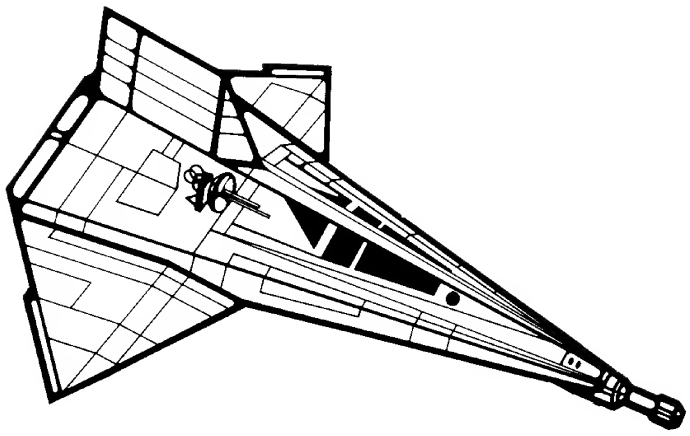
The attract mode begins when power is applied to the game, after a play or high-score mode, or after self-test. This mode repeats every 30 seconds. It ends only when a credit is entered or when self-test begins.

The screen displays one of four possible pictures in this mode. The first picture displays the single-player high-score table for approximately ten seconds. The words SCORE, FUEL, and GAME OVER appear. The words INSERT COIN and the coin mode appear if no coin(s) or not enough coins are inserted. The number of credits may show, if any. During this time the 1-player and 2-player red light-emitting diode (LED) lights flash.

Table 1-5 Gravitar™ High-Score Lists

Depending on the highest score, one of eight list names appears above the table of initials.

Name of List	Points
FLUNKY	0-20,000
GUNNER	20,001-40,000
CO-PILOT	40,001-80,000
PILOT	80,001-100,000
ACE PILOT	100,001-200,000
KILLER PILOT	200,001-400,000
PONTIUS PILATE	400,001-800,000
GOTTA-BE-LUCKY	above 800,000



The second picture spells GRAVITAR in expanding and contracting letters. It lasts approximately nine seconds.

The third picture lasts about two seconds. The screen shows a solar system with a player's blue space ship in the center at home base. All planets and their respective bonus point values are visible. ATARI MCMLXXXII copyright message appears in the center of this picture, and the number of credits (if any). DANGER appears above the death star. The ship flies toward the easiest planet in the upper right part of the screen.

The fourth picture in this mode is a full-screen view of planet terrain with the player's blue space ship appearing at the top center of the screen. The ship travels in the scrolling, zooming terrain until it crashes or is shot down. The words SHOOT BUNKERS, TRACTOR FUEL, SCORE, FUEL, and number of credits (if any) are displayed.

Game play begins when the correct credit(s) is entered and the 1- or 2-player button(s) is pressed.

3. Play Mode

The play mode begins in the first solar system with the player's blue ship in the center of the screen at home base. There are four regular planets plus a fifth red alien planet and a death star arranged clockwise around the screen in increasing order of difficulty. The planets are worth 2,000, 4,000, 6,000, and 8,000 points with a value of 9,000 points on the alien planet. The positions of the alien planet and the death star vary in the second and third solar systems. After the first solar system all planets are valued at 9,000 points. The death star, located near home base, is the center of gravity in each solar system. Colliding with it results in the loss of one life, and the player returns to home base.

The words SCORE (with current total score), FUEL (running total of original 10,000-point fuel supply), and BONUS (decreasing point value of planet under attack) appear at the top of the screen throughout game play.

Player controls consist of LEFT ROTATE, RIGHT ROTATE, FIRE, THRUST, and TRACTOR/SHIELD yellow pushbuttons. Use FIRE to shoot targets. A player has four shells that must hit a target or must travel their full distance in order to be reloaded. TRACTOR/SHIELD retrieves fuel with a tractor beam and shields the ship from alien shots. The TRACTOR/SHIELD does not prevent the ship from crashing into land or alien ships. TRACTOR/SHIELD and THRUST decrease the player's fuel supply. Using these controls together decreases the fuel supply even faster.

Blue fuel cells are positioned just below a planet's surface. There are two, three, or four fuel cells per planet terrain (depending on level of game play). Each cell beamed aboard ship with TRACTOR is worth 2,500 fuel units.

If the player's ship is above the highest point on some planet terrains, flying alien rammers attack him. Shooting a rammer scores 100 points.

If the player gets too close to a shooting alien ship, he is involved in a one-on-one space dogfight, and either he or the alien ship must die. If the player is victorious, he returns to the solar system at his original spot; if the alien ship wins, the player loses a life and returns to home base.

Red alien bunkers appear on each planet. There are two, four, six, or eight bunkers per surface (depending on the difficulty of the planet). The bunkers fire shots to protect the fuel cells. Exploding a bunker scores 250 points. Exploding all bunkers in a solar system displays a MISSION COMPLETE message.

The word SUPERBONUS and the number of superbonus points appear in the middle of the screen only after a completed mission on the first planet in the first solar system. These superbonus points are awarded on the basis of initial difficulty of the first planet sucessfully completed. The higher the bonus point value of the planet attacked, the higher the superbonus awarded. No superbonus points are awarded for attacking the 2,000-point (easiest) planet or for attacking the four regular planets in consecutive order of difficulty.

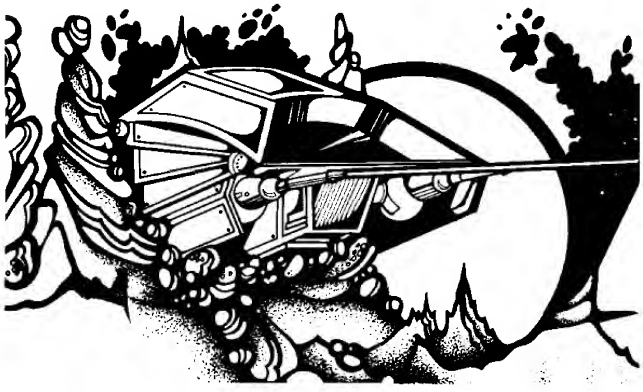


Table 1-6 Gravitar™ Scoring

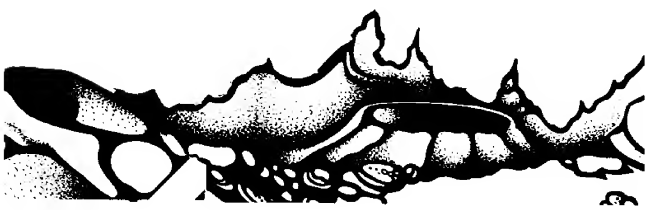
Planet Bonus*	Superbonus**
9,000	20,000
8,000	12,000
6,000	6,000
4,000	2,000
2,000	0
Obstacles	**Points**
Red bunker	250
Rammer	100
Alien Ship	100

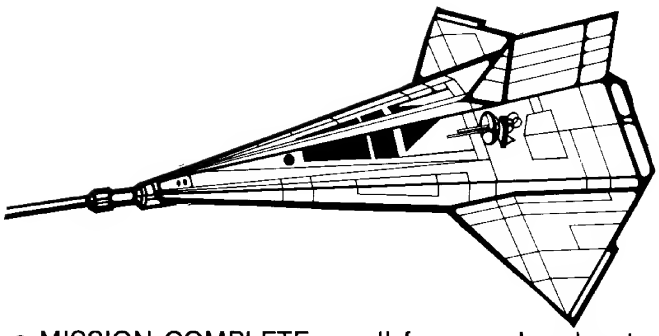
*Constantly decreases with elapsed game time
**Awarded after first MISSION COMPLETE achieved

A player may fly to any planet he chooses. The number beside each planet is the starting number of bonus points for that planet. Entering a planet causes the distinct planet terrain to appear. To get maximum points, the player must shoot all alien bunkers and see MISSION COMPLETE at the top of the screen. A player may exit a planet at any time; he does not have to stay any longer than he wishes.

The red alien planet (worth 9,000 points) is home for red alien ships that must be shot down or avoided. The alien planet looks the same in every solar system: terrain consists of a spiral tunnel with a reactor at its end. Under a decrementing timer, the player must maneuver through the tunnel without hitting the walls and shoot the reactor. (Hitting the walls or not escaping in time places the player back at home base.) Shooting the reactor will make it glow and pulsate. Then the player must escape before the timer reaches zero. (In the next solar systems, the timer of the alien planet decreases by two seconds, and there are shooting bunkers to overcome.) Completing the mission on the alien planet places the player in the next solar system with an additional 7,500 fuel points.

Gravitar progresses by waves of planets (new solar systems). Successfully destroying the reactor and escaping from the red alien planet, or achieving





a MISSION COMPLETE on all four regular planets places the player in the next solar system (next level of game play). The four levels of game play are described as follows:

a. Regular gravity
b. Negative gravity
c. Regular gravity with invisible landscape and maximum difficulty
d. Negative gravity with invisible landscape and maximum difficulty

Alien ship speed and firing frequency, rammer speed, bunker firing frequency, and bonus points are all based on time elapsed in game play. Both regular and negative gravity increase, depending on the initial planet bonus level.

The game ends when all lives are used up or when player is out of fuel. Then the screen briefly displays the words SCORE, FUEL, PLAYER 1 (or 2), GAME OVER.

4. High-Score Mode

This mode begins if a player has earned one of the eight highest scores. The player has one minute to enter his initials. Letters of the alphabet increment with LEFT ROTATE and decrement with RIGHT ROTATE pushbuttons. Select letters with the TRACTOR/SHIELD pushbutton. To reset the high-score table, power the game *off* and then *on*, or enter and end the self-test mode (this does not erase the top three scores).

5. Hints for Game Play

- Develop skill for controlling the space ship in regular and negative gravity.
- Beam up fuel cells with TRACTOR/SHIELD.
- Attack the red alien planet first for maximum challenge and 20,000 bonus points! Completion of this planet immediately places a player in the next solar system where all planets are worth 9,000 bonus points.
- Attack more difficult planets early in the game for higher bonus points.
- Many planet terrains have safe areas or "blind spots" from which the player can safely shoot at bunkers.

Troubleshooting

This game tests itself when the self-test switch is set to the *on* position. If there is a failure, the game produces audiovisual aids to help you find the failing portion of the game. The self-test procedure included in Chapter 1 will help you decide if the game is or isn't working properly. The expanded self-test procedures in this chapter are included to help the qualified electronic technician troubleshoot the game.

Chapter 2

A. Comments on Troubleshooting

When troubleshooting, first determine the symptom(s) of the failure. After determining the symptom, look over the wiring diagram and determine what assemblies could cause the failure. Could it be caused by the power supply, Regulator/Audio II PCB, or the video display?

The next step is to check all harness wires and connectors to the suspected failing assembly. If you find no harness or connector problem, substitute an assembly known to be good for the suspected failing assembly. If the game functions properly, you have successfully isolated the failure. If it doesn't, repeat the procedure with another assembly.

When you have isolated the failing assembly, you must troubleshoot that assembly and make the necessary repairs. If the video display is failing, we suggest that a qualified video display technician handle the troubleshooting and repair. If the power supply or Regulator/Audio II PCB is failing, troubleshooting and repair are relatively simple, as these assemblies are not too complicated. If a game PCB is failing, troubleshooting and repair depends on your understanding of the operation of the PCB.

To effectively troubleshoot a game PCB, learn as much as you can about the PCB. The diagrams in the *Schematic Package* (included with the game) show the functions of the circuitry. Again, while troubleshooting the PCB, first determine the symptom of the failure, then locate the suspected area on the schematic diagram.

The *Schematic Package* has signatures printed in red at the proper test-node points for PCB memory devices. For example, to determine if the self-test ROM is functioning properly, perform signature analysis with the ATARI® CAT Box. The *Schematic Package*. contains a complete description of signature analysis using the CAT Box.

A glossary of schematic signal descriptions is included in the *Schematic Package*. Each signal description states if the signal is hardware- or software-generated, where it is generated, where it goes, and what it does. We suggest you use this glossary to become more familiar with the operation of the game PCB.

B. Self-Test Procedure

To enter Self-Test, set the self-test switch to the *on* position. Press FIRE and then 1-player start. If the test passes, the screen goes blank for a few seconds and then displays the picture below. See *Chapter 1, Section F, Self-Test Procedure* for a complete description of this picture.

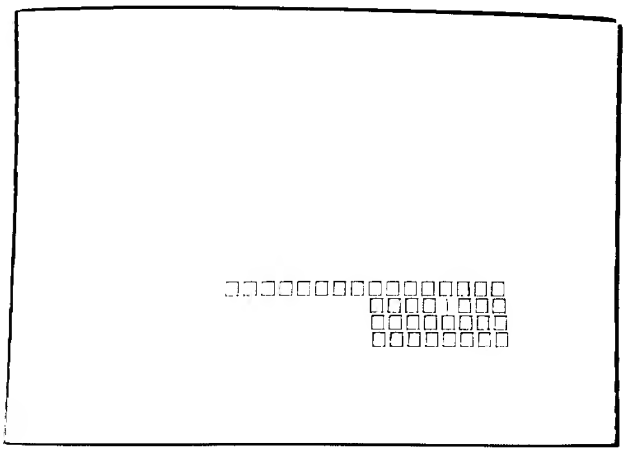


Figure 2-1 Self-Test Screen 1 Test Passes

NOTE

This procedure does not test the coin door lockout coils and coin counter. If the lockout coils do not energize when the game is on, suspect the lockout coil wiring, coin door harness, game PCB harness, latch R9, or driver Q2 of the game PCB. Troubleshoot using the game schematics.

SCREEN 1:

RAM failure is indicated by a sound and, if possible, an *R* displayed in the top center of the screen. Count the tones. One or two tones indicates RAM failure at game PCB location N/P1. Three or four tones indicate RAM failure at game PCB location K7.

Tone	Failing RAM Location on Game PCB
1st or 2nd	N/P1
3rd or 4th	K7

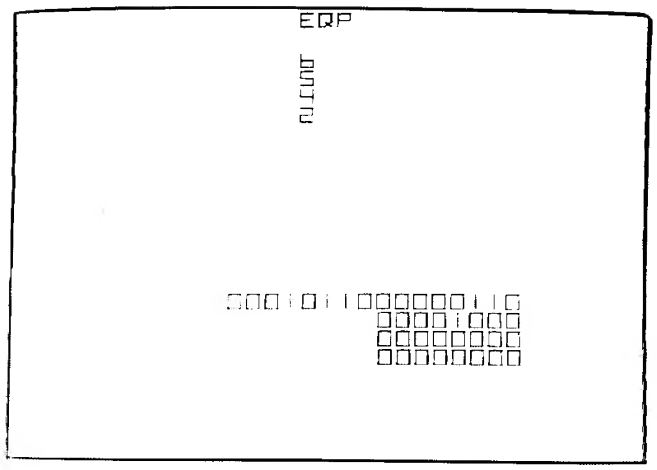


Figure 2-2 Self-Test Screen 1 Test Fails

ROM failure is indicated by one or more vertically arranged numbers displayed on the top half of the screen (see *Figure 2-2*). The bad ROM and its location are listed as follows:

Screen Display	Failing ROM Location on Game PCB
0 *	L7
1 *	M/N7
2 *	N/P7
3	R7
4	D1
5	E/F1
6	H1
7	J1
8	K/L1
9 **	M1

*If this ROM is bad you will hear a constant low tone, and the program may be unable to display a screen image.
**If this ROM is bad, the screen may be blank.

EAROM or CUSTOM I/O CHIP failure is indicated by one letter in the top center of the sceen. Identify the failure with the table below.

Letter Displayed	Location on Game PCB
E	EAROM at M2
P	Custom I/O chip at C/D3
Q	Custom I/O chip at B3

SWITCH failure is indicated by the associated *0* not changing to a *1* on the screen and no sound when the switch is activated. Troubleshoot using the information in *Chapter 3, Section B,* and game schematics.

SOUND failure is indicated by no sound. Check the volume control levels on the utility panel, or troubleshoot using the game schematics.

To see the remaining self-test screens (2 through 8), press the coin switch on the utility panel for each screen.

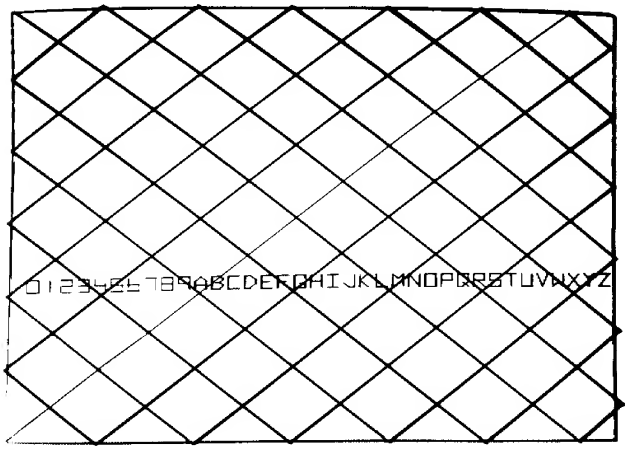
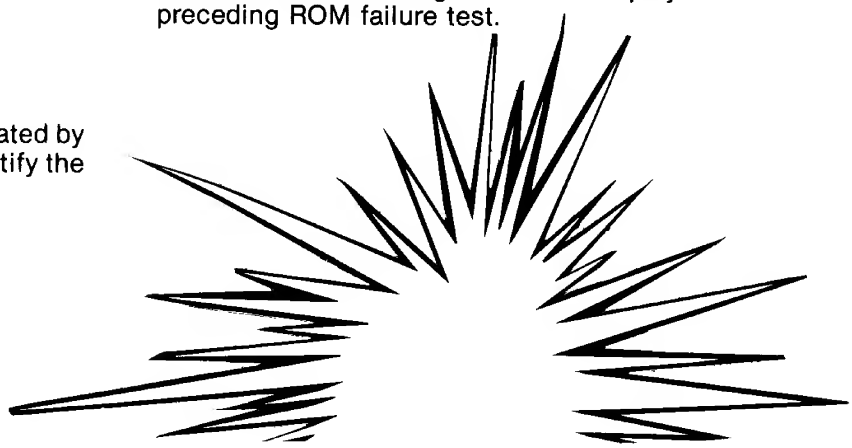


Figure 2-3 Self-Test Screen 2

SCREEN 2:

A white diagonal grid pattern and a complete character set appear on the screen (see *Figure 2-3*). The edges of the grid pattern should touch the sides of the screen. If the display is not centered, symmetrical, or the proper size, adjust the X SIZE, Y SIZE, X CTR, Y CTR, X LIN, OR Y LIN pots on the game PCB (refer to the *Schematic Package*). If the characters are incorrect, check again for a *2* displayed in the preceding ROM failure test.



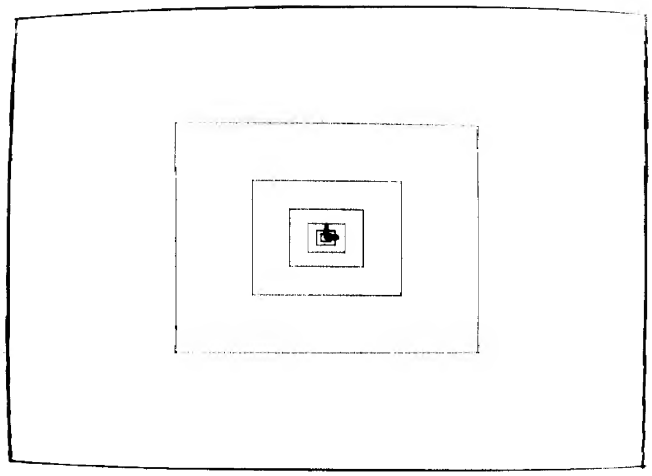


Figure 2-4 Self-Test Screen 3

SCREEN 3:

A white box of decreasing size appears during this test. The box should shrink smoothly. There are seven stages, each with a tone. This pattern tests the binary and linear scaling circuitry. Troubleshoot using the game schematics.

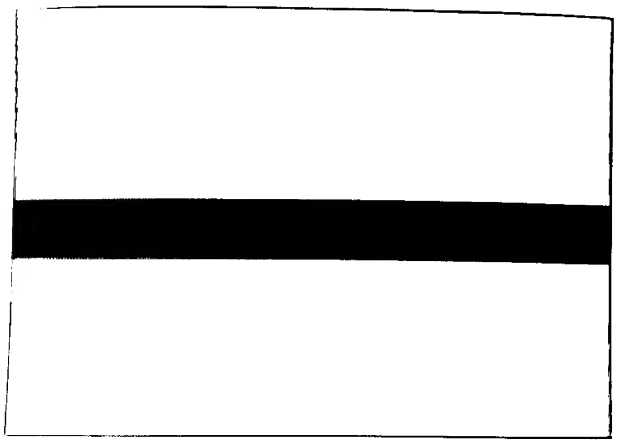


Figure 2-5 Self-Test Screen 4

SCREEN 4:

A series of horizontal lines are visible in the middle of the screen. This is a raster test, used by the manufacturer only, to set the color levels.

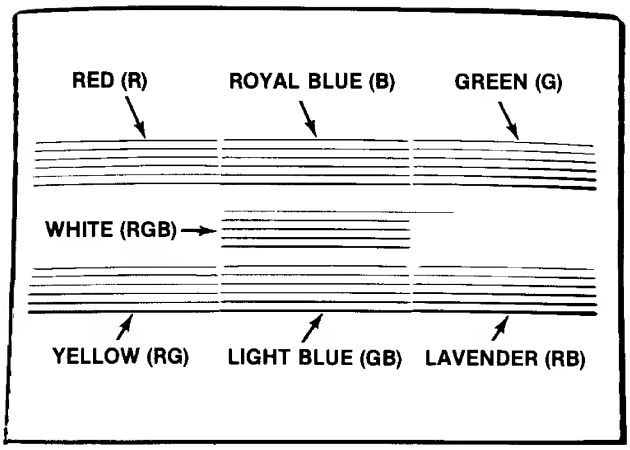


Figure 2-6 Self-Test Screen 5

SCREEN 5:

This test checks the seven screen colors and six intensities of each color (see *Figure 2-6*). If the intensities do not progress from dim at the top of each color group to bright at the bottom, there is a problem in the Z-axis of the game PCB or the video display. Use this pattern for tracking adjustments (refer to the color X-Y display manual).

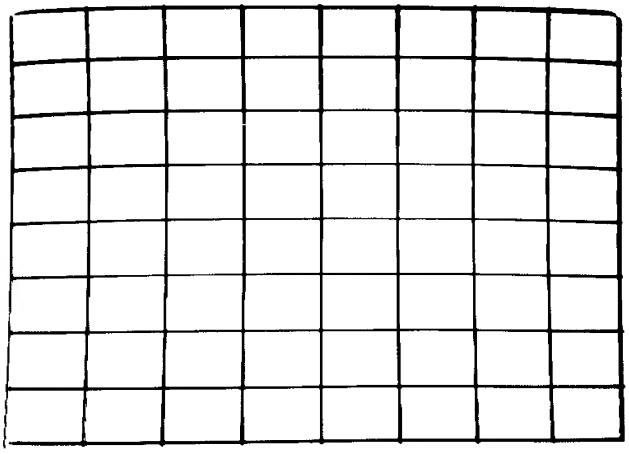


Figure 2-7 Self-Test Screen 6

SCREEN 6:

A grid pattern touches the corners of the video display (see *Figure 2-7*). Press the 1-player start button to change colors. Use this pattern for purity and convergence adjustments (refer to the color X-Y display manual).

VECTOR-GENERATOR DIAGNOSTIC PROGRAM

The diagnostic program is controlled by switches 2, 3, and 4 in the 4-toggle option switch bank at location P10/11 on the game PCB. This group of switches lets you choose one of six tests.

These tests provide recurring sequences to make it easy for you to troubleshoot the vector-generator circuitry. The tests and their respective option switch settings are as follows:

Test	Action	Settings of 4-Position DIP Switch at P10/11		
		4	3	2
Test 1	Press WDDIS every 4 msec (blank screen)	Off	Off	Off
Test 2	Test vector-generator halt instruction every .55 msec (blank screen)	On	Off	Off
Test 3	Test vector-generator long vector (and halt instruction) every 8.2 msec	Off	On	Off
Test 4	Test vector-generator jump instruction (and long vector and halt instructiion) every 8.2 msec	On	On	Off
Test 5	Test vector-generator short vector instruction (and all of Test 4) every 8.6 msec	Off	Off	On
Test 6	Test vector-generator JSRL/RTSL instruction (and all of Test 5) every 10.2 msec	On	Off	On
Test 2	Blank screen	Off	On	On
Test 2	Blank screen	On	On	On

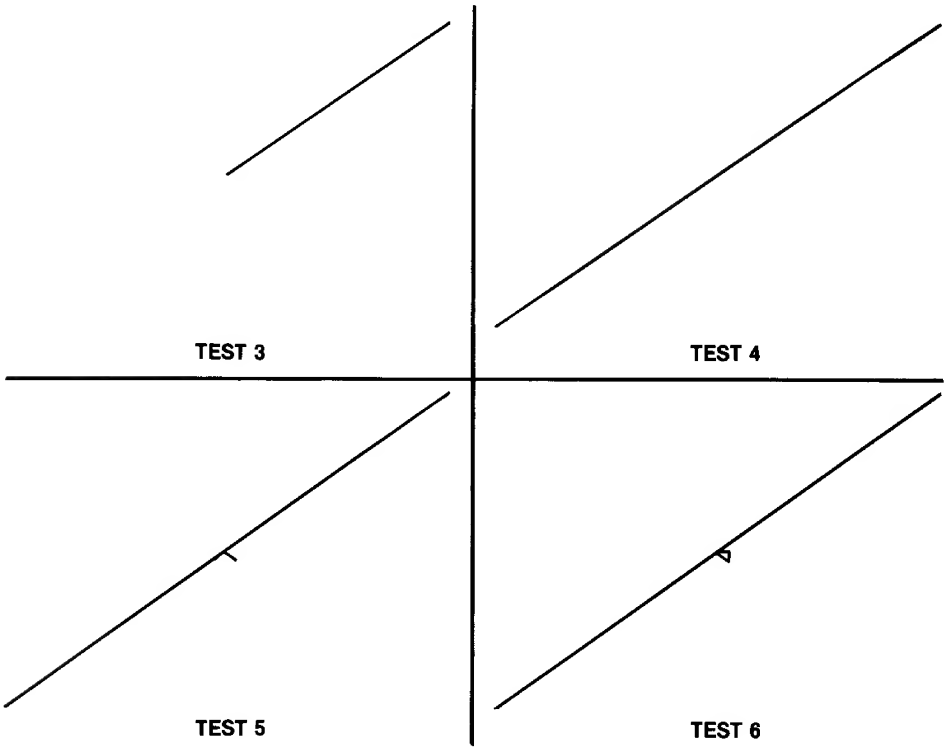


Figure 2-8 Screen 7 : Self-Test Screens During Signature Analysis

Press the coin switch while pressing the 2-player start button. The screen will either be blank or display vectors, depending on settings of the switch toggles at location P10/11 on the game PCB (see *Figure 2-8*).

To exit from this screen, set the self-test switch to *off* or press RESET on the game PCB.

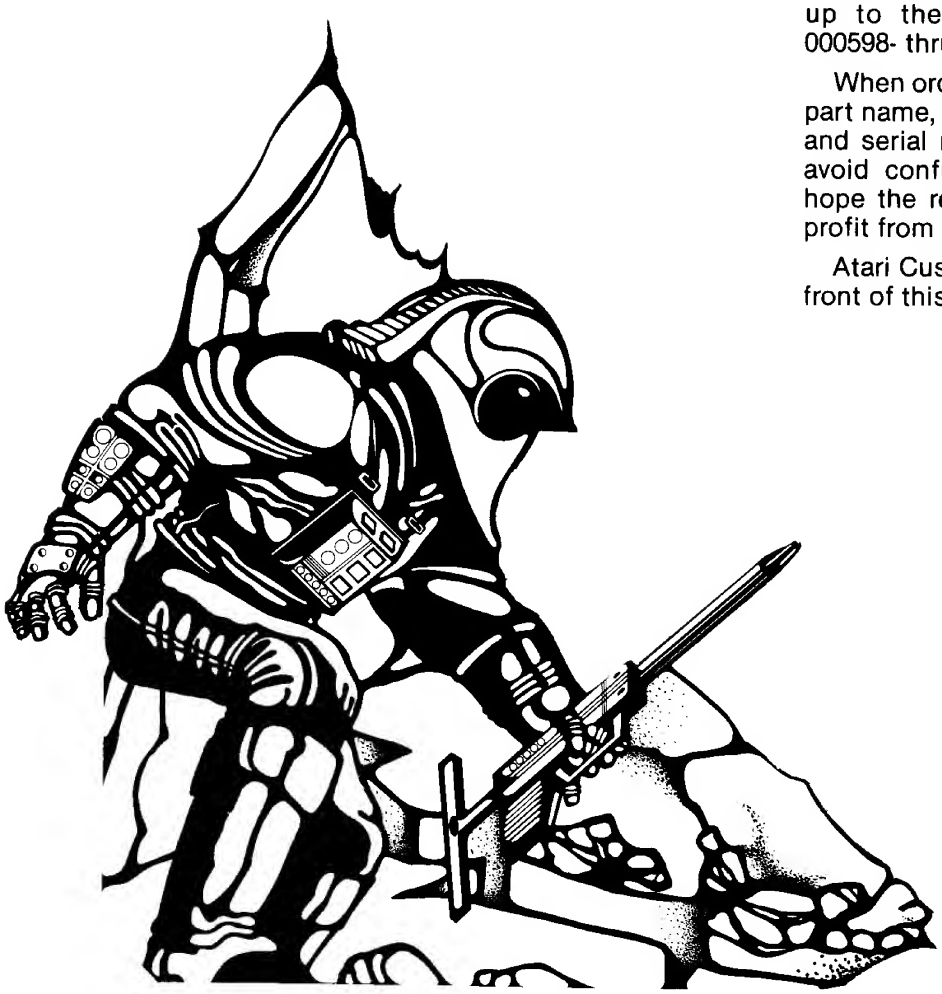
Maintenance, Repair and Parts

This chapter details maintenance and repair information and provides information you need to order parts for your Gravitar™ game. Please note that **common hardware has been deleted** from most of the parts lists. Common hardware includes screws, nuts, washers, bolts, and the like.

The parts lists are arranged in alphanumeric order. For example, all A- prefix numbers come first. Following these are numbers in sequence evaluated up to the hyphen, namely 00- thru 99-, then 000598- thru approximately 190000-.

When ordering parts, please give the part number, part name, applicable figure number of this manual, and serial number of your game. This will help to avoid confusion and mistakes in your order. We hope the results will be less downtime and more profit from your game.

Atari Customer Service numbers are listed in the front of this manual for your convenience.



Chapter 3

A. Cabinet-Mounted Assemblies

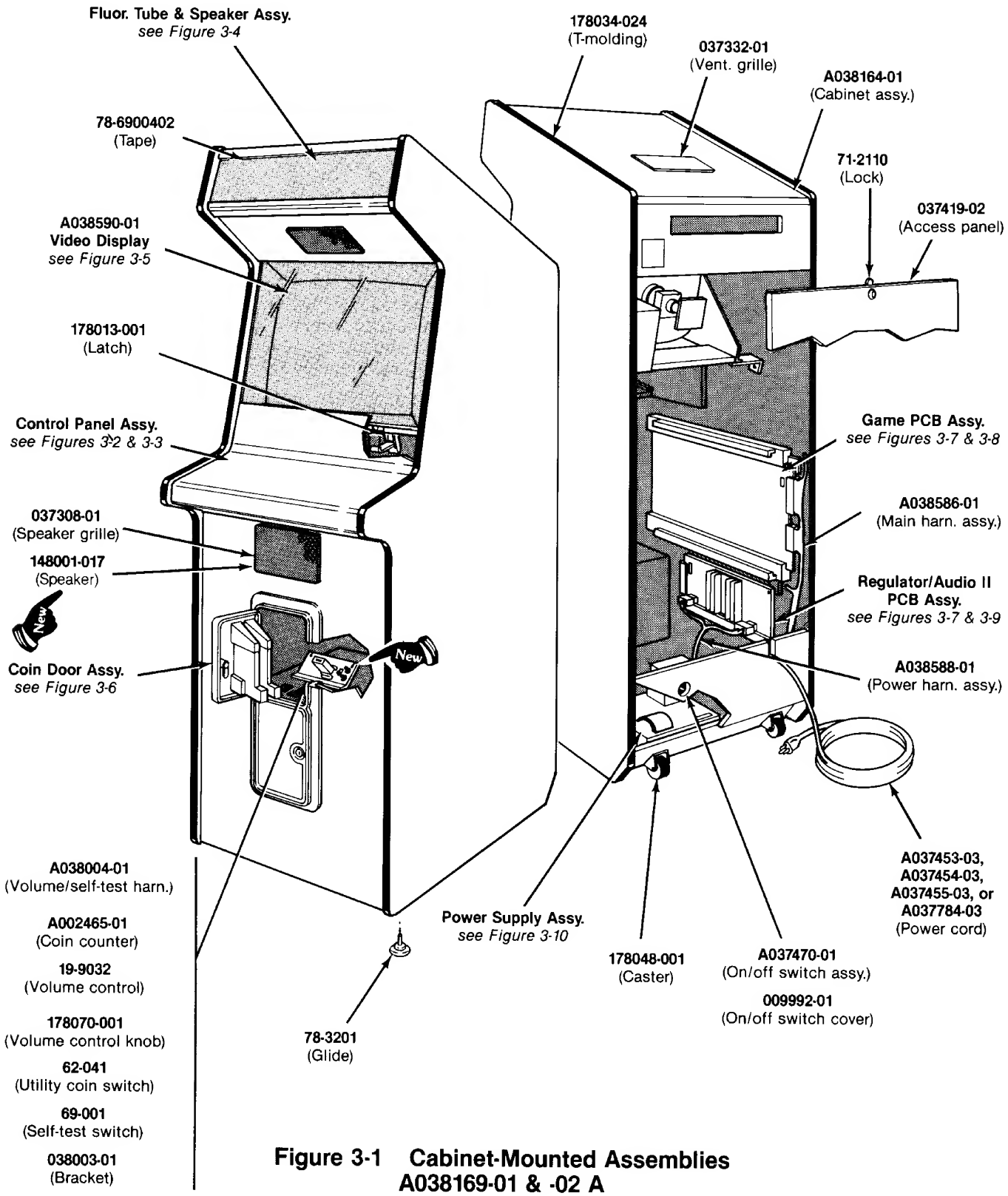


Figure 3-1 Cabinet-Mounted Assemblies A038169-01 & -02 A

Figure 3-1 Cabinet-Mounted Assemblies, continued
Parts List

Part No.	*Description (Reference Designations and Locations in Bold)*
A002465-01	Coin Counter
A037453-03	Strain-Relief Power Cord *(U.S. and Canada)*
A037455-03	Strain-Relief Power Cord *(Australia and New Zealand)*
A037470-01	Power On/Off Switch/Mounting Plate Assembly
A037784-03	Strain-Relief Power Cord *(United Kingdom, Ireland, Lebanon, Saudi Arabia, India, Hong Kong, Singapore, Egypt, Nigeria, Republic of South Africa, Zimbabwe)*
A038004-01	Harness for Volume Control/Self-Test Switch/Coin Counter Assembly
A038164-01	Cabinet Assembly *(includes glides and PCB retainers, but not the rear access panel)*
A038586-01	Main Harness Assembly
A038588-01	Power Harness Assembly
A038590-01	19-Inch Wells-Gardner Color X-Y Video Display Assembly
	The following four items are the technical information supplements to this game:
SP-206	Gravitar Schematic Package
ST-206-01	Gravitar Label with Self-Test Procedure and Option Switch Settings
TM-183	Service Manual for 19-Inch Wells-Gardner Color X-Y Display
TM-206	Gravitar Operation, Maintenance, and Service Manual
19-9032	Volume Control
62-041	SPDT Momentary-Contact Pushbutton Utility Coin Switch with Black Cap
69-001	DPDT Self-Test Switch
71-2110	Lock Mechanism *(for rear access panel)*
78-3201	Adjustable Glide
78-6900402	Vinyl Foam Single-Coated Adhesive Tape, ¼-Inch Wide x ⅛-Inch Thick
009992-01	On/Off Switch Cover
037308-01	Speaker Grille
037332-01	Ventilation Grille
037419-02	Rear Access Panel *(does not include lock)*
038003-01	Bracket for Volume Control, Self-Test Switch, and Coin Counter(s)
038091-01	Molded Coin Box *Acceptable substitute is part no. A037491-01*
178013-001	Spring Draw Latch
178034-024	¾-Inch Black Plastic T-Molding
178048-001	2-Inch Rigid Caster
178070-001	Volume Control Knob

B. The Control Panel

WARNING

Before removing or repairing any switch on the control panel, **unplug the game.**

To Open the Control Panel:

1. Open the coin door. Reach up through the opening to the top of the control panel and release the spring-draw latches. (You may also release the spring-draw latches from the back of the game cabinet after opening the rear access panel.)
2. Close the coin door.
3. Lift up on the control panel at the top edge and tilt it toward you. There is foam tape on the display shield, which cushions the shield and prevents liquids from entering the cabinet interior. Make sure this tape is in good condition.

To Repair Leaf Switches:

1. Adjust the leaf switches for a narrow gap. When a switch button is depressed, the resulting wiping action of the cross-bar contacts provides a self-cleaning feature. **Don't burnish the contacts.** To clean them, use electrical contact cleaner.
2. To replace a leaf switch, remove the screw with a Phillips-head screwdriver.
3. To replace the switch button, turn the stamped nut with a wrench in a counterclockwise direction as seen from inside the control panel. The ring on the outside of the control panel should not spin.
4. To reinstall the switch, reconnect the harness wires as shown in the *Schematic Package, Game Wiring Diagram.* Make certain the colored wires are routed to their matching colored tabs on the switch.

To Repair LED Start and SELECT Switches:

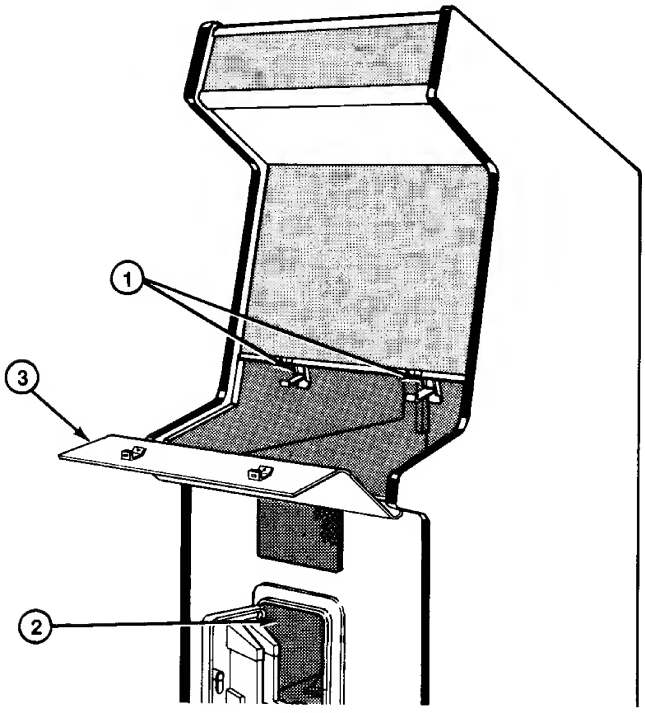
These switches have a very low failure rate. If a switch should ever be suspect, first test it using the following directions.

To Test LED Switch:

I. Remove the wires from the suspected switch.
2. Attach the leads of an ohmmeter to normally open and common contacts.
3. Check contacts (push and release the switch button) for closed and open continuity.
4. If the contacts do not operate sharply or always remain closed or open, replace the switch.

To Replace LED Switch:

1. Remove all wires from the faulty switch.
2. Turn the switch counterclockwise while holding the black cone-shaped bushing on the outside of the control panel.
3. Install a new switch using the reverse procedure.
4. Reconnect the harness wires as shown in *Figure 3-2.*



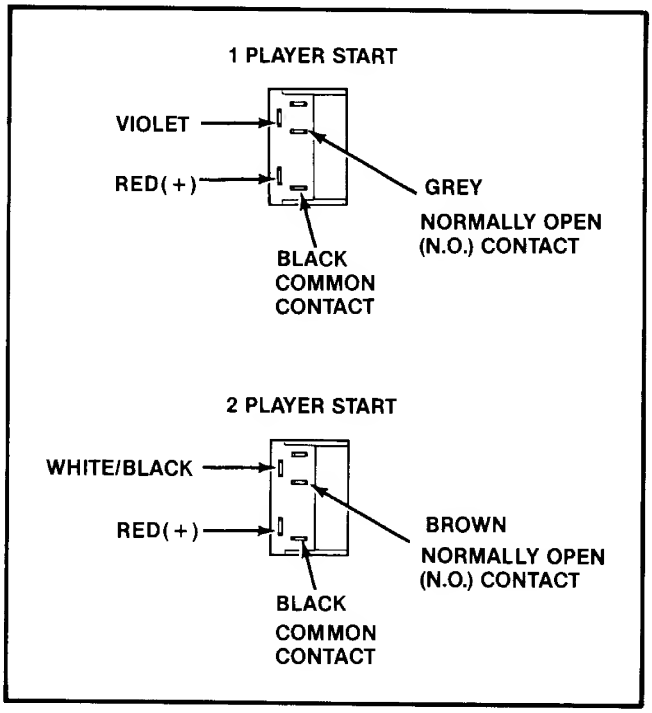


Figure 3-2 Control Panel

WARNING

Players may receive an electric shock if this control panel is not properly grounded! After servicing any parts on the panel, check that the ground wire is firmly attached to the metal tab on the inside of the control panel. Only **then** should you lock up the game.

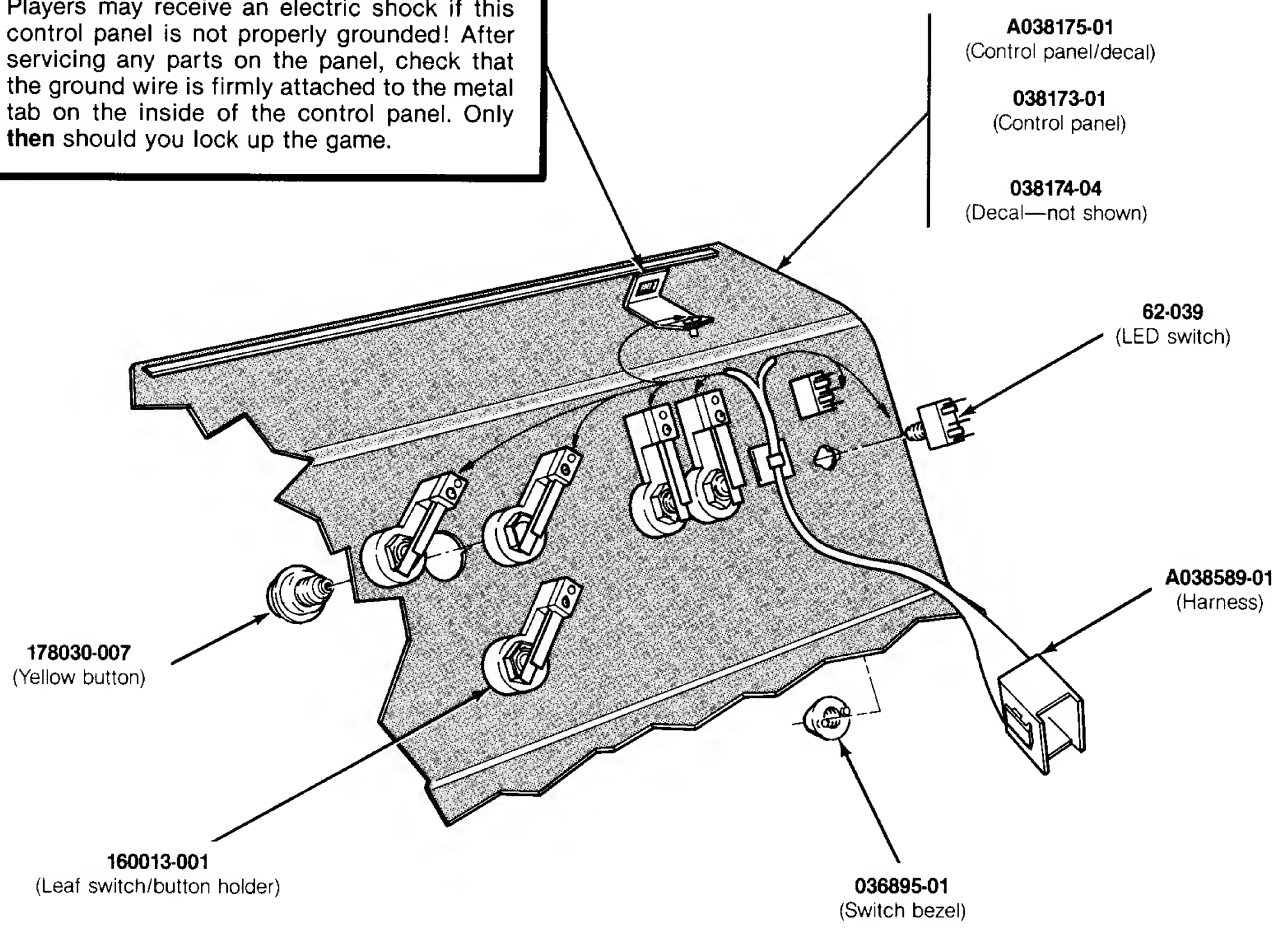


Figure 3-3 Control Panel Assembly A038176-01 A

Parts List

Part No.	*Description (Reference Designations and Locations in Bold)*
A038175-01	Control Panel with Decal
A038589-01	Control Panel Harness Assembly
62-039	SPDT Momentary Pushbutton Start Switch with Red Light-Emitting Diode
036895-01	Black Molded Switch Bezel
038173-01	Control Panel
038174-04	Control Panel Decal
160013-001	Leaf Switch and Button Holder *(leaf switch only is part no. 160012-001)*
178030-007	Yellow Pushbutton Assembly

C. Fluorescent Tube and Speaker

WARNING

Before removing or repairing the fluorescent tube or speaker, **unplug the game.**

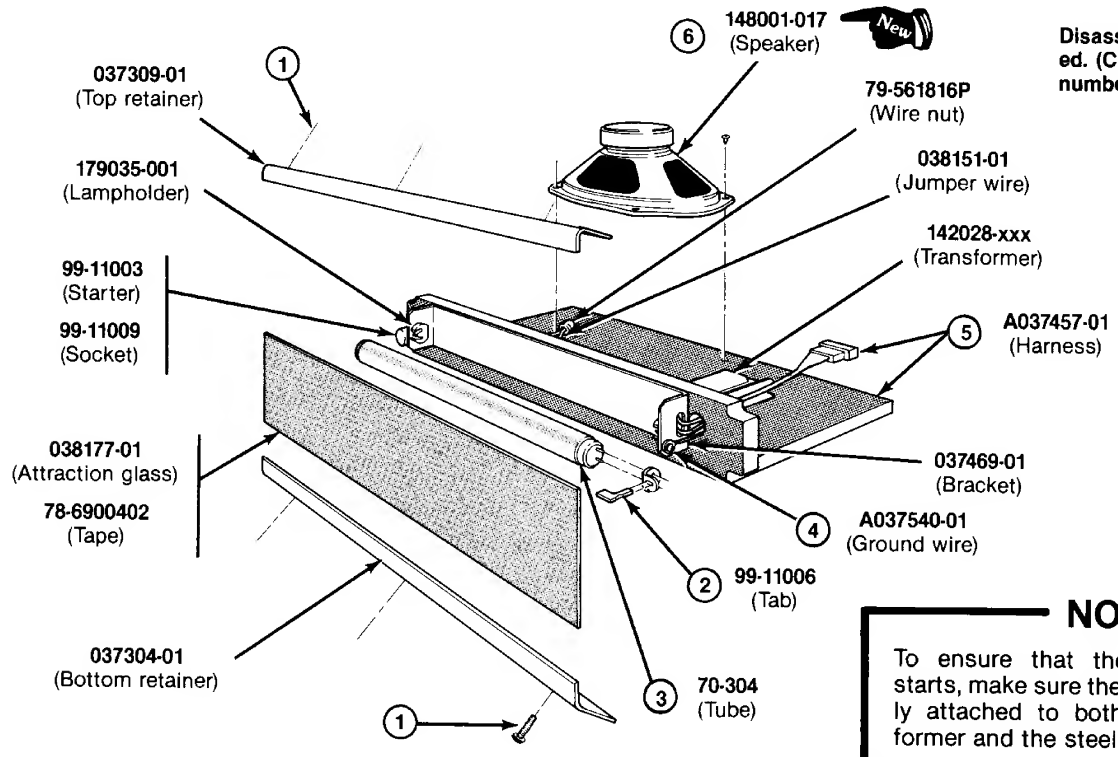
If you drop a fluorescent tube and it breaks, *it will implode!* Shattered glass can fly six feet or more from the implosion. Use care when replacing any fluorescent tube.

To Replace Fluorescent Tube:

1. Remove the three sets of hardware that secure the upper attraction panel retainer to the cabinet. *Loosen* the three sets of hardware that secure the lower retainer to the cabinet. Lift the attraction panel up and out of its lower retainer.
2. Remove the cardboard locking tab at each end of the tube. Slightly rotate the tube up or down and carefully remove it from the lampholders.
3. Replace with a new tube. Do not snap the tube in vigorously—*you may break it, causing an implosion!* Replace the locking tabs.
4. Check that the green ground wire is securely attached to the large metal bracket and the ballast transformer on the wood panel. If the tube is not grounded, it may not start.

To Replace Cabinet Speakers:

5. **Upper speaker.** Remove upper attraction glass. Slide the fluorescent tube and speaker board partially out of the cabinet. Turn it sideways to unplug the 5-pin harness connector. Remove the board from the cabinet.
6. Unplug the two plug-in connectors on the speaker. Note that the white wire (+) connects on the side marked with a painted dot. Remove the hardware that attaches the speaker to the board. Replace the speaker, reinstall the speaker board, and reconnect the harness.
7. **Lower speaker.** Open the rear access panel. Unplug the two plug-in connectors on the speaker. Note that the white wire (+) connects on the side marked with a painted dot. Remove the hardware that attaches the speaker to the cabinet. Install the new speaker, and replace the hardware and connectors.



Disassemble in the order indicated. (Circled numbers match the numbered instructions.)

NOTE

To ensure that the fluorescent tube starts, make sure the ground wire is firmly attached to both the ballast transformer and the steel lamp bracket.

Figure 3-4 Fluorescent Tube and Speaker A038161-01 & -02 A

Figure 3-4 Fluorescent Tube and Speaker A038161-01 & -02 A Parts List

Part No.	*Description (Reference Designations and Locations in Bold)*
A037457-01	Tube and Speaker Harness Assembly
A037540-01	Ground Wire with Ring Lug
70-304	18-Inch, 15-W, Cool White Fluorescent Tube
78-6900402	Vinyl Foam Single-Coated Adhesive Tape, ¼-inch Wide x ⅛ inch Thick
79-561816P	Spring-Connector Wire Nut for 16- to 18-Gauge Wires
99-11003	Fluorescent Lamp Starter
99-11006	Fluorescent Lamp Locking Tab *(tab consists of two pieces)*
99-11009	Starter Socket
037304-01	Bottom Attraction Glass Retainer
037309-01	Top Attraction Glass Retainer
038151-01	15-Inch Jumper Wire
038177-01	Attraction Glass with Graphics
037469-01	Steel Lamp Bracket
142028-001	60 Hz, 118 V, Ballast Transformer *(used on A038161-01 assembly)*
142028-002	50 Hz, 118 V, Ballast Transformer *(used on A038161-02 assembly)*
148001-017	6 x 9-Inch, 8 Ω, 6-Ounce Oval Shielded High-Fidelity Speaker
179035-001	2-Pin Fluorescent Lampholder

D. Video Display

To Remove Wells-Gardner Color X-Y Display:

1. Open the rear access panel and unplug the 15-pin display harness connector. Remove the hardware that secures the display chassis to the metal bracket.
2. Open the control panel (see *Figure 3-2).*
3. Lift up on the glass shield. Slide the retainer clip off the wood cleat and remove it through the cutout. Now remove the glass shield by sliding it down and out of the cabinet.
4. Remove the cardboard bezel.
5. Remove the four sets of hardware that secure the display frame to the wood shelf.
6. Carefully pull the display out through the front of the cabinet. Place it on a soft mat in a protected location.

WARNING

SHOCK HAZARD

The following procedure should only be performed by a *qualified service technician.* Before removing or repairing the video display, **unplug the game.** As an extra precaution, we highly recommend you **discharge the high voltage** from the picture tube.

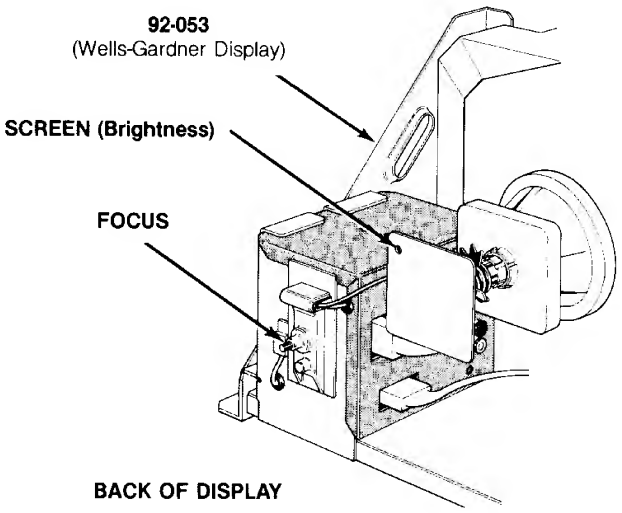
High voltages may exist in any video display, even with power disconnected. Use extreme caution and do not touch electrical parts of the display yoke area with your hands or with metal objects in your hands!

IMPLOSION HAZARD

If you drop the display and the picture tube breaks, *it will implode!* Shattered glass and the yoke can fly six feet or more from the implosion. Use care when replacing any display.

Figure 3-5 Video Display
Parts List

Part No.	*Description (Reference Designations and Locations in Bold)*
	Wells-Gardner Display A038590-01
A038593-01	Wells-Gardner Interconnect Assembly
92-053	19-Inch Wells-Gardner Color X-Y Video Display
038181-01	Video Display Support Bracket
037303-01	Display Shield
037322-01	Display Bezel
037330-01	Display Shield Retainer Clip



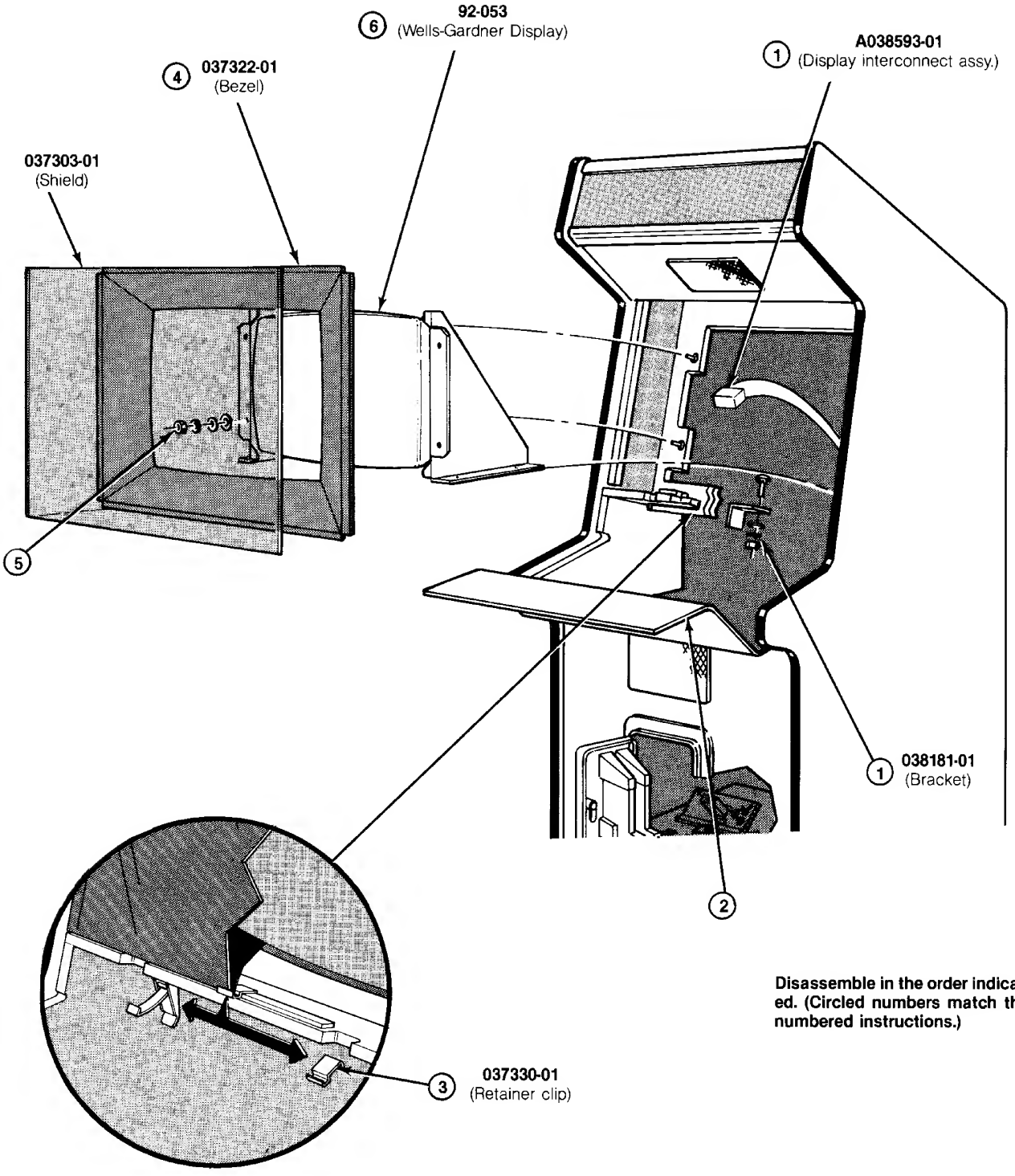


Figure 3-5 Video Display, continued
A038590-01

E. Coin Door

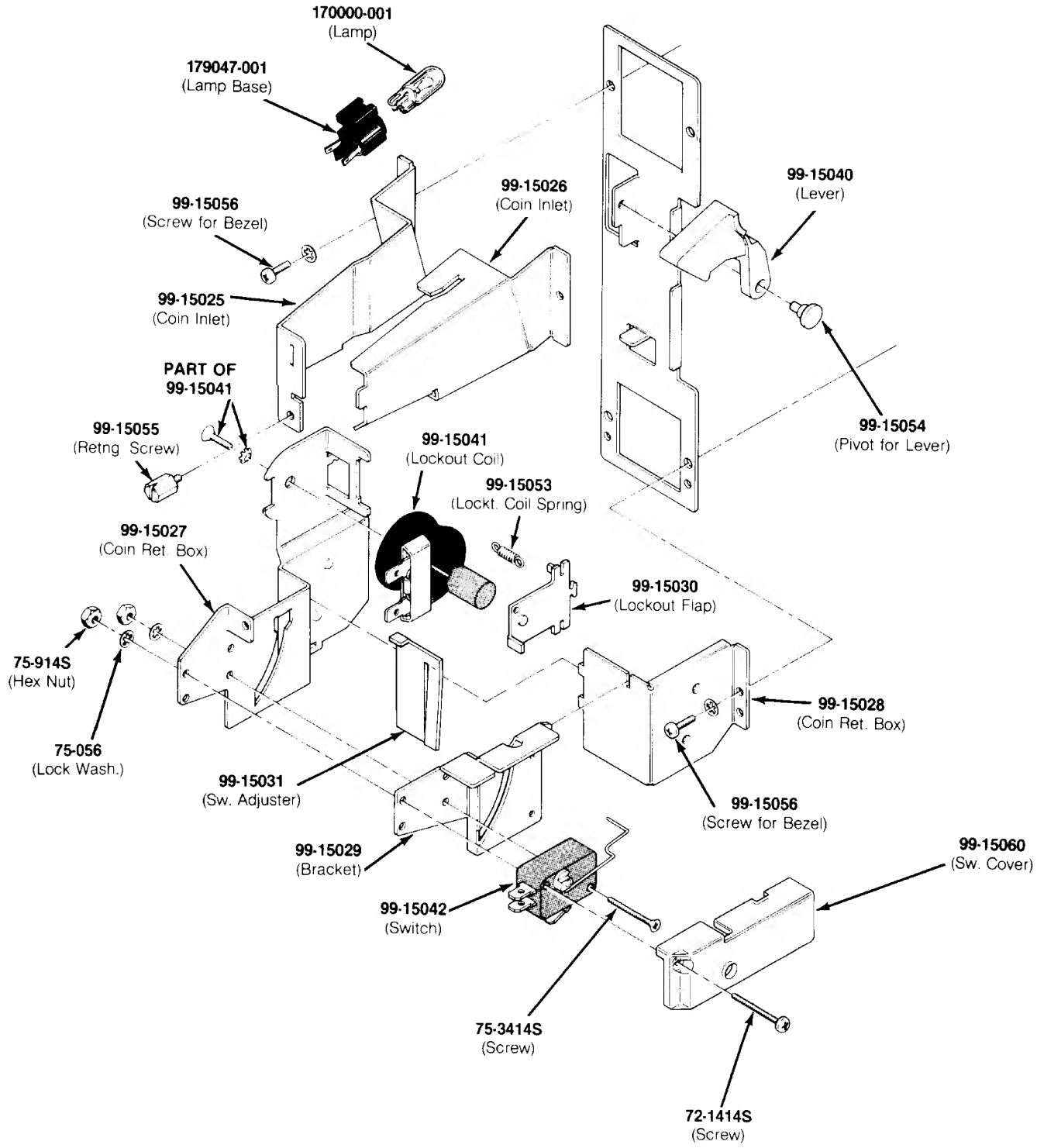
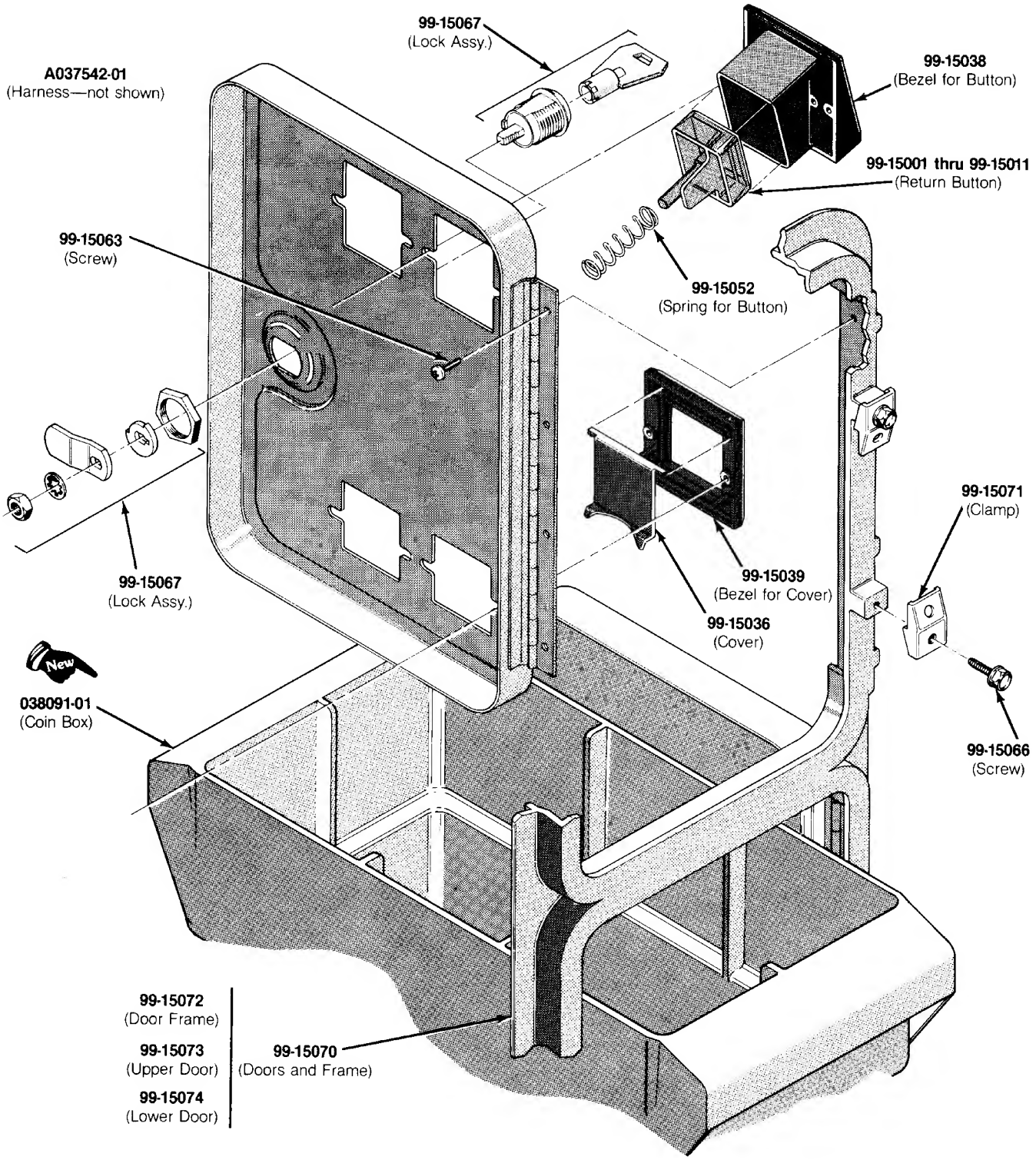


Figure 3-6 Vertically Mounted Coin Door
A037619-xx D



A037619-01 — U.S. 25¢/25¢ Coin Door
A037619-02 — U.S. 50¢/50¢ Coin Door
A037619-03 — Canadian 25¢/25¢ Coin Door
A037619-04 — British 10 P/10 P Coin Door
A037619-05 — British 10 P/50 P Coin Door
A037619-06 — British 20 P/50 P Coin Door
A037619-07 — Australian 20¢/20¢ Coin Door
A037619-08 — German 1 DM/1 DM Coin Door
A037619-09 — German 2 DM/1 DM Coin Door
A037619-10 — German 2 DM/5 DM Coin Door
A037619-11 — German 1 DM/5 DM Coin Door
A037619-12 — 5 Fr/5 Fr Coin Door
A037619-13 — Swiss 1 Fr/1 Fr Coin Door
A037619-14 — French 1 Fr/1 Fr Coin Door
A037619-15 — French 2 Fr/1 Fr Coin Door
A037619-16 — Swedish 1 Kr/1 Kr Coin Door
A037619-17 — Spanish 25 Pts/25 Pts Coin Door
A037619-18 — Italian 100 L/100 L Coin Door
A037619-19 — Hong Kong $1/$1 Coin Door
A037619-20 — Japanese 100Y/100Y Coin Door

Figure 3-6 Vertically Mounted Coin Door, continued
A037619-xx D

Figure 3-6 Vertically Mounted Coin Door, continued
Parts List

Part No.	*Description*
038091-01	Coin Box *(Not included in assembly) Acceptable substitute is part number A037491-01.*
A037542-01	Harness Assembly
72-1414S	#4-40 × 7/8-Inch Cross-Recessed Pan-Head Steel Machine Screw
75-056	#6 Internal-Tooth Zinc-Plated Steel Lock Washer
75-914S	#4-40 Steel Machine Hex Nut
75-3414S	#4-40 × 7/8-Inch 82° Cross-Recessed Flat-Head Steel Machine Screw
99-15001	Coin Return Button with U.S. 25¢ Price Plate
99-15002	Coin Return Button with U.S. $1 Price Plate
99-15003	Coin Return Button with German 1 DM Price Plate
99-15004	Coin Return Button with German 2 DM Price Plate
99-15005	Coin Return Button with German 5 DM Price Plate
99-15006	Coin Return Button with Belgian 5 Fr Price Plate
99-15007	Coin Return Button with French 1 Fr Price Plate
99-15008	Coin Return Button with Japanese 100 Yen Price Plate
99-15009	Coin Return Button with British 10 Pence Price Plate
99-15010	Coin Return Button with Australian 20¢ Price Plate
99-15011	Coin Return Button with Italian 100 Lire Price Plate
99-15023	Base Plate
99-15025	Left Half of Coin Inlet
99-15026	Right Half of Coin Inlet
99-15027	Side Plate of Coin Return Box
99-15028	Base Plate of Coin Return Box
99-15029	Switch Bracket
99-15030	Flap for Lockout Coil *(U.S. 25¢)*
99-15031	Switch Adjuster
99-15036	Metal Coin Return Cover
99-15038	Bezel for Coin Return Button
99-15039	Metal Bezel for Coin Return Cover
99-15040	Coin Return Lever
99-15042	Coin Switch for U.S. 25¢
99-15052	Spring for Coin Return Button
99-15054	Pivot for Coin Return Lever
99-15055	Retaining Screw
99-15056	#4-40 × 5/16-Inch Cross-Recessed Pan-Head Steel Machine Screw
99-15060	Switch Cover
99-15063	Screw for Hinge
99-15066	Screw for Clamp
99-15067	Lock Assembly
99-15068	Lockout Coil
99-15069	Spring for Lockout Coil
99-15070	Doors and Frame
99-15071	Clamp for Frame
99-15072	Door Frame
99-15073	Upper Door
99-15074	Lower Door
170000-001	6.3V Miniature Wedge-Base Incandescent Lamp
171006-035	Metal Coin Mechanism
179047-001	Lamp Base

F. Printed-Circuit Boards

WARNING

Before removing or repairing any printed-circuit board, **unplug the game.**

To Remove Printed-Circuit Boards:

1. Open the rear access panel.
2. For the *game PCB,* unplug the two edge connectors. Remove the screw and spacer that secure the PCB to the cabinet. **Carefully** slide the PCB straight out of its slots. Be careful not to twist the board, as this may loosen connections or components. Replace or repair as required.
3. For the *Regulator/Audio II PCB,* disconnect the five small harness connectors on this board.
4. Remove the screw and spacer that secure the Regulator/Audio II PCB to the cabinet, and carefully remove the board from its slot. Do not twist the board, as this may loosen connections or components. Replace or repair as required and reinstall.
5. Make sure that the connectors on the PCB are properly plugged in. Note that they are keyed to fit only one way. If they do not slip on easily, do not force them. **A reversed connector may damage your game** and void the warranty.
6. Replace the hardware that secures the Regulator/Audio II PCB to the cabinet wall. Reinstall the plug-in connectors to the PCB.
7. Close and lock the rear access panel.
8. Ensure that the operation of the game is correct by performing the self-test. Performing self-test is very important when you repair a PCB.

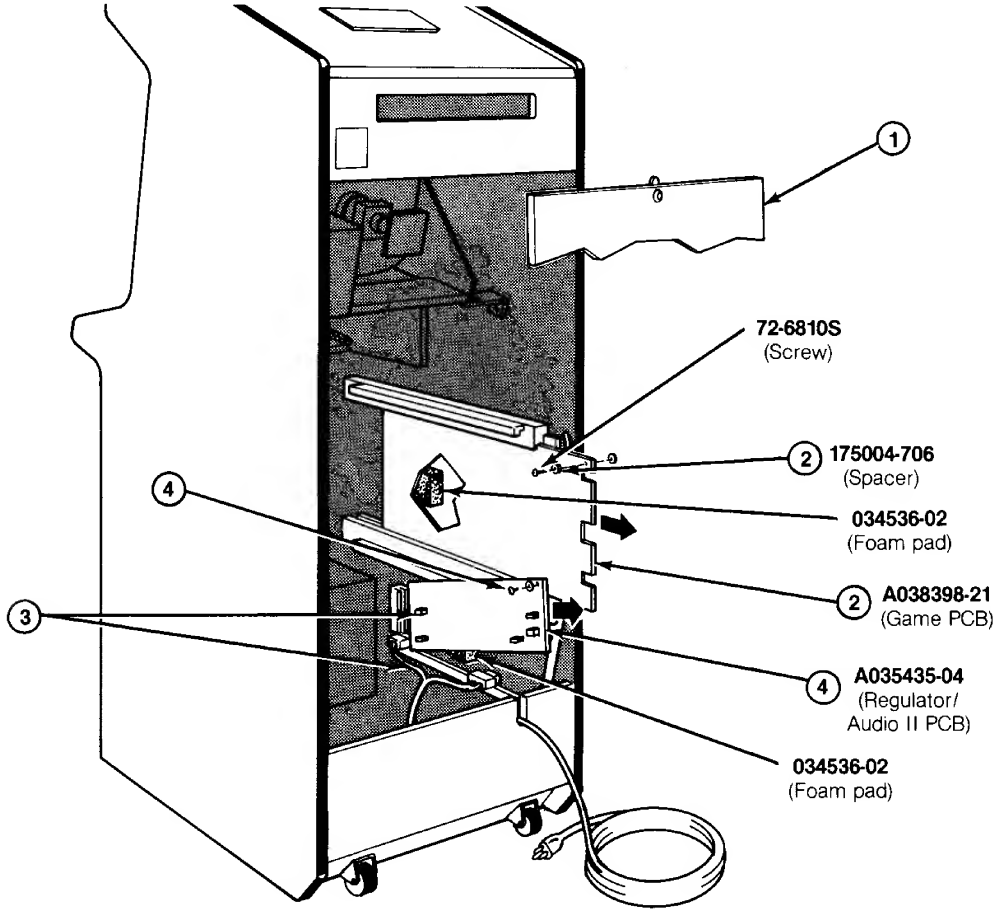


Figure 3-7 Printed-Circuit Board Removal

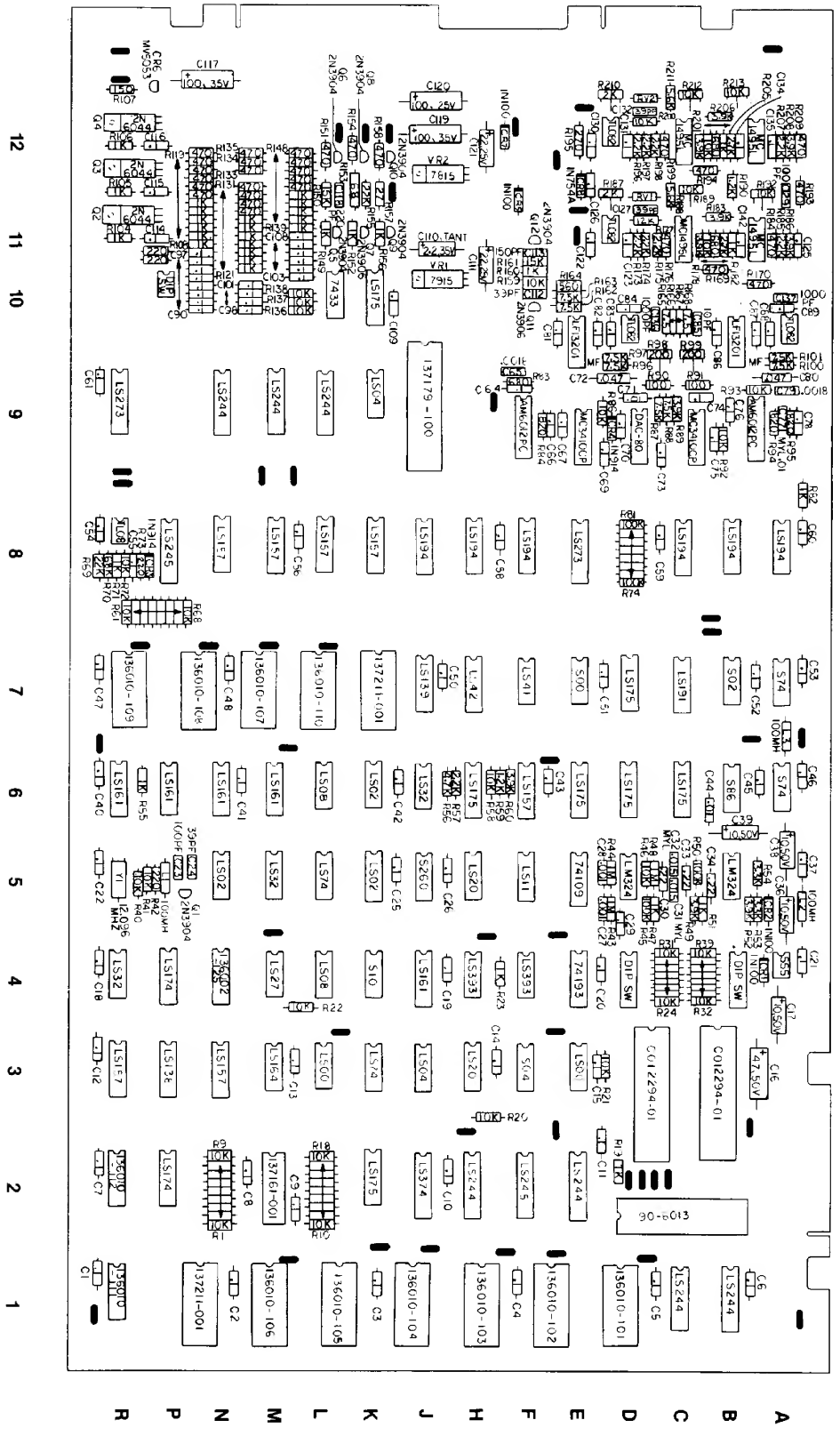


Figure 3-8 Gravitar™ Game PCB Assembly A038398-21 & -22 A

Figure 3-8 Gravitar™ Game PCB Assembly, continued Parts List

Part No.	Description (Reference Designations and Locations in Bold)
	For A038398-21 Version Only
27-102182	0.0018 μF, ± 10%, 1 kV Radial-Lead Ceramic-Disc Capacitor **(C79)**
110000-103	10 kΩ, ± 5%, ¼ W Resistor **(R86, 92, 93)**
122002-104	0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor **(C67, 69, 74, 75)**
137160-003	10-Bit Digital-to-Analog Converter **(C9, E9)**
	For A038398-22 Version Only
21-101103	0.01 μF, ± 10%, 100 V, Radial-Lead Epoxy-Dipped Capacitor **(C77)**
27-102182	0.0018 μF, ± 10%, 1 kV, Ceramic-Disc Radial-Lead Capacitor **(C65)**
110000-681	680 Ω, ± 5%, ¼ W Resistor **(R83)**
110000-821	820 Ω, ± 5%, ¼ W Resistor **(R84, 94, 95)**
122002-104	0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor **(C64, 66, 76, 78)**
137158-002	12-Bit Digital-to-Analog Converter **(A/B9, F9)**
	For A038398-21 & -22 Versions
19-315103	10 kΩ Vertical PCB-Mounting Cermet Trimpot **(R189, 192, 212, 213)** *Acceptable substitute is part no. 119002-103.*
19-315202	2 kΩ Vertical PCB-Mounting Cermet Trimpot **(R187, 210)** *Acceptable substitute is part no. 119002-202.*
19-315501	200 Ω Vertical PCB-Mounting Cermet Trimpot **(R98, 99)** *Acceptable substitute is part no. 119002-501.*
21-101153	0.015 μF, ± 10%, 100 V Radial-Lead Epoxy-Dipped Mylar Capacitor **(C31, 32)**
24-250226	22 μF, 25 V Electrolytic Fixed Axial-Lead Capacitor **(C111, 121)**
24-350107	100 μF, 35 V Aluminum Electrolytic Fixed Axial-Lead Capacitor **(C117, 119, 120)**
24-500106	10 μF, 50 V Aluminum Electrolytic Fixed Axial-Lead Capacitor **(C17, 36, 38, 39)**
24-500476	47 μF, 50 V Aluminum Electrolytic Fixed Axial-Lead Capacitor **(C16)**
31-1N100	Type-1N100, 100 V Switching Diode **(CR1, 2, 5, 7)**
31-1N914	Type-1N914, 75 V Switching Diode **(CR3, 4)**
33-2N3906	Type-2N3906 PCB Switching and Amplifying Transistor **(Q7, 11)**
34-2N3904	Type-2N3904, 60 V, 1 W NPN Transistor **(Q1, 5, 6, 8-10, 12)**
34-2N6044	Type-2N6044 Darlington NPN Transistor **(Q2-4)**
37-555	Type-555 Integrated Circuit **(A4)**
37-1495	Type-MC1495L Integrated Circuit **(A/B11, A/B12, C11, C12)**
37-7433	Type-7433 Integrated Circuit **(L10)**
37-13201	Type-LF13201 Integrated Circuit **(B10, E10)**
37-74109	Type-74109 Integrated Circuit **(E5)**
37-74193	Type-74193 Integrated Circuit **(E4)**
37-LM324	Type-LM324 Integrated Circuit **(B5, D5)**
37-74LS00	Type-74LS00 Integrated Circuit **(E3, L3)**
37-74LS02	Type-74LS02 Integrated Circuit **(K5, K6, N5)**
37-74LS04	Type-74LS04 Integrated Circuit **(J3, K9)**
37-74LS08	Type-74LS08 Integrated Circuit **(L4, L6)**
37-74LS14	Type-74LS14 Integrated Circuit **(F7)**
37-74LS20	Type-74LS20 Integrated Circuit **(H3, H5)**
37-74LS27	Type-74LS27 Integrated Circuit **(M4)**
37-74LS32	Type-74LS32 Integrated Circuit **(J6, M5, R4)**

[Continued on next page]

Figure 3-8 Gravitar™ Game PCB Assembly, continued
Parts List

Part No.	*Description (Reference Designations and Locations in Bold)*
37-74LS42	Type-74LS42 Integrated Circuit **(H7)**
37-74LS74	Type-74LS74 Integrated Circuit **(K3, L5)**
37-74LS139	Type-74LS139 Integrated Circuit **(J7)**
37-74LS157	Type-74LS157 Integrated Circuit **(F6, K8, L8, M8, N3, N8, R3)**
37-74LS161	Type-74LS161 Integrated Circuit **(J4, M6, N6, P6, R6)**
37-74LS164	Type-74LS164 Integrated Circuit **(M3)**
37-74LS174	Type-74LS174 Integrated Circuit **(P2, P4)**
37-74LS175	Type-74LS175 Integrated Circuit **(C6, D6, D7, E6, H6, K2, K10)**
37-74LS191	Type-74LS191 Integrated Circuit **(C7)**
37-74LS194	Type-74LS194 Integrated Circuit **(A8, B8, C8, F8, H8, J8)**
37-74LS244	Type-74LS244 Integrated Circuit **(B1, C1, E2, H2, L9, M9, N9)**
37-74LS245	Type-74LS245 Integrated Circuit **(F2, P8)**
37-74LS273	Type-74LS273 Integrated Circuit **(E8, R9)**
37-74LS374	Type-74LS374 Integrated Circuit **(J2)**
37-74LS393	Type-74LS393 Integrated Circuit **(F4, H4)**
37-74S00	Type-74S00 Integrated Circuit **(E7)**
37-74S02	Type-74S02 Integrated Circuit **(B7)**
37-74S04	Type-74S04 Integrated Circuit **(F3)**
37-74S74	Type-74S74 Integrated Circuit **(A6, A7)**
37-74S260	Type-74S260 Integrated Circuit **(J5)**
37-7815	+ 15 V Voltage Regulator **(VR2)**
37-7915	− 15 V Voltage Regulator **(VR1)**
37-TL082CP	Type-TL082 Integrated Circuit **(A10, D10, D/E11, D/E12, R8)**
38-MV5053	Type-MV5053 Light-Emitting Diode **(CR6)**
41-3003	100 μH, ±10%, Hot-Molded Plastic Fixed R.F. Choke **(L1-3)** *Acceptable substitute is part no. 141002-001.*
66-114P1T	4-Station Single-Throw, Dual-Inline-Package Bit Switch **(P10)**
66-118P1T	8-Station Single-Throw, Dual-Inline-Package Bit Switch **(B4, D4)**
72-6810S	#8 x ⅝-Inch Phillips-Head Screw *(secures PCB to cabinet)*
79-42C22	22-Contact Medium-Insertion-Force Integrated Circuit Socket **(M2)**
79-42C24	24-Contact Medium-Insertion-Force Integrated Circuit Socket **(D1, E/F1, H1, J1, K7, K/L1, L7, M1, M/N7, N/P1, N/P7, R7)**
79-42C40	40-Contact Medium-Insertion-Force Integrated Circuit Socket **(B3, C2, C/D3, J9)**
81-4302	Nylon Snap-In Fastener
90-6013	Microprocessor **(C2)**
034536-02	Foam Pad
038178-03	Dual-Slotted PCB Retainer
110000-101	100 Ω, ±5%, ¼ W Resistor **(R90, 91)**
110000-102	1 kΩ, ±5%, ¼ W Resistor **(R19, 23, 47, 51, 55, 71, 82, 104-106, 108-113, 121-127, 139-143, 149, 152, 156, 160, 182, 204)**
110000-103	10 kΩ, ±5%, ¼ W Resistor **(R1-18, 20-22, 24-41, 46, 58, 61-68, 72, 136-138, 159, 179, 200, 202)**
110000-104	100 kΩ, ±5%, ¼ W Resistor **(R45, 50, 74-81)**
110000-105	1 MΩ, ±5%, ¼ W Resistor **(R43, 44, 48)**
110000-122	1.2 kΩ, ±5%, ¼ W Resistor **(R59, 190)**
110000-123	12 kΩ, ±5%, ¼ W Resistor **(R177)**
110000-151	150 Ω, ±5%, ¼ W Resistor **(R107)**
110000-153	15 kΩ, ±5%, ¼ W Resistor **(R150, 161)**

[Continued on next page]

Figure 3-8 Gravitar™ Game PCB Assembly, continued Parts List

Part No.	Description (Reference Designations and Locations in Bold)
110000-221	220 Ω, ±5%, ¼ W Resistor **(R42, 73, 102, 103)**
110000-222	2.2 kΩ, ±5%, ¼ W Resistor **(R57, 173-175, 185, 196-198, 207)**
110000-223	22 kΩ, ±5%, ¼ W Resistor **(R69, 155)**
110000-270	27 Ω, ±5%, ¼ W Resistor **(R157)**
110000-272	2.7 kΩ, ±5%, ¼ W Resistor **(R181, 205)**
110000-332	3.3 kΩ, ±5%, ¼ W Resistor **(R53, 54)**
110000-392	3.9 kΩ, ±5%, ¼ W Resistor **(R49, 52, 60, 89, 178, 183, 186, 201, 206, 208)**
110000-471	470 Ω, ±5%, ¼ W Resistor **(R114-119, 128-131, 133-135, 144-148, 151, 154, 158, 169, 170, 176, 184, 193, 194, 199, 209)**
110000-472	4.7 kΩ, ±5%, ¼ W Resistor **(R56)**
110000-561	560 Ω, ±5%, ¼ W Resistor **(R164)**
110000-562	5.6 kΩ, ±5%, ¼ W Resistor **(R188, 211)**
110000-680	68 Ω, ±5%, ¼ W Resistor **(R153)**
110000-681	680 Ω, ±5%, ¼ W Resistor **(R180, 203)**
110000-683	68 kΩ, ±5%, ¼ W Resistor **(R70)**
110001-271	270 Ω, ±5%, ½ W Resistor **(R195)**
110003-752	7.5 kΩ, ±1%, ⅛ W Resistor **(R87, 88, 96, 97, 100, 101, 162, 163, 165-168)**
110004-001	Voltage Dependent Resistor **(RV1, 2)**
121007-473	0.047 μF, ±10%, 50 V, Radial-Lead Epoxy-Dipped Polycarbonate Capacitor **(C72, 80)**
122000-225	2.2 μF, ±10%, 35 V Tantalum Capacitor **(C110)**
122002-102	0.001 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor **(C27, 28)**
122002-104	0.1 μF, 50 V, Ceramic-Disc Radial-Lead Capacitor **(C1-15, 18-22, 25, 26, 29, 35, 37, 40-43, 45-63, 70, 73, 81-84, 86-101, 103-109, 114-116, 122-126, 130, 131, 134, 135)**
122005-103	0.01 μF, 25 V, Ceramic-Disc Radial-Lead Capacitor **(C44, 71)**
122008-224	0.22 μF, 25 V, Ceramic-Disc Radial-Lead Capacitor **(C30, 33, 34)**
128002-100	10 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor **(C85)**
128002-101	100 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor **(C23, 129)**
128002-102	1000 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor **(C136, 137)**
128002-151	150 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor **(C113)**
128002-221	220 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor **(C118)**
128002-390	39 pF, 100 V, Radial-Lead Epoxy-Dipped Mica Capacitor **(C24, 112, 127, 132)**
131002-001	Type-1N754A, 6.8 V Zener Diode **(CR8)**
136002-125	Programmable Read-Only Memory **(N4)**
136010-101	Programmable Read-Only Memory **(D1)**
136010-102	Programmable Read-Only Memory **(E/F1)**
136010-103	Programmable Read-Only Memory **(H1)**
136010-104	Programmable Read-Only Memory **(J1)**
136010-105	Programmable Read-Only Memory **(K/L1)**
136010-106	Programmable Read-Only Memory **(M1)**
136010-107	Programmable Read-Only Memory **(M/N7)**
136010-108	Programmable Read-Only Memory **(N/P7)**
136010-109	Programmable Read-Only Memory **(R7)**
136010-110	Programmable Read-Only Memory **(L7)**
136010-111	Programmable Read-Only Memory **(R1)**
136010-112	Programmable Read-Only Memory **(R2)**
137002-001	Type-74S86 Integrated Circuit **(B6)**

[Continued on next page]

Figure 3-8 Gravitar™ Game PCB Assembly, continued
Parts List

Part No.	*Description (Reference Designations and Locations in Bold)*
137149-001	Type-74LS11 Integrated Circuit **(F5)**
137159-001	8-Bit Digital-to-Analog Converter **(D9)**
137161-001	Electrically-Alterable Read-Only Memory **(M2)**
137177-001	Type-74LS138 Integrated Circuit **(P3)**
137179-001	Address Controller **(J9)**
137211-001	Random-Access Memory **(N/P1, K7)**
137236-001	Type-74S10 Integrated Circuit **(K4)**
144000-001	12.096 MHz, ±.005% Crystal **(Y1)**
175004-706	#8 Spacer *(secures PCB to cabinet)*
179051-002	Test Point *Acceptable substitute is part no. 020670-01.*
C012294-01	Audio I/O N-Channel MOS/LSI Custom Chip **(B3, C/D3)**

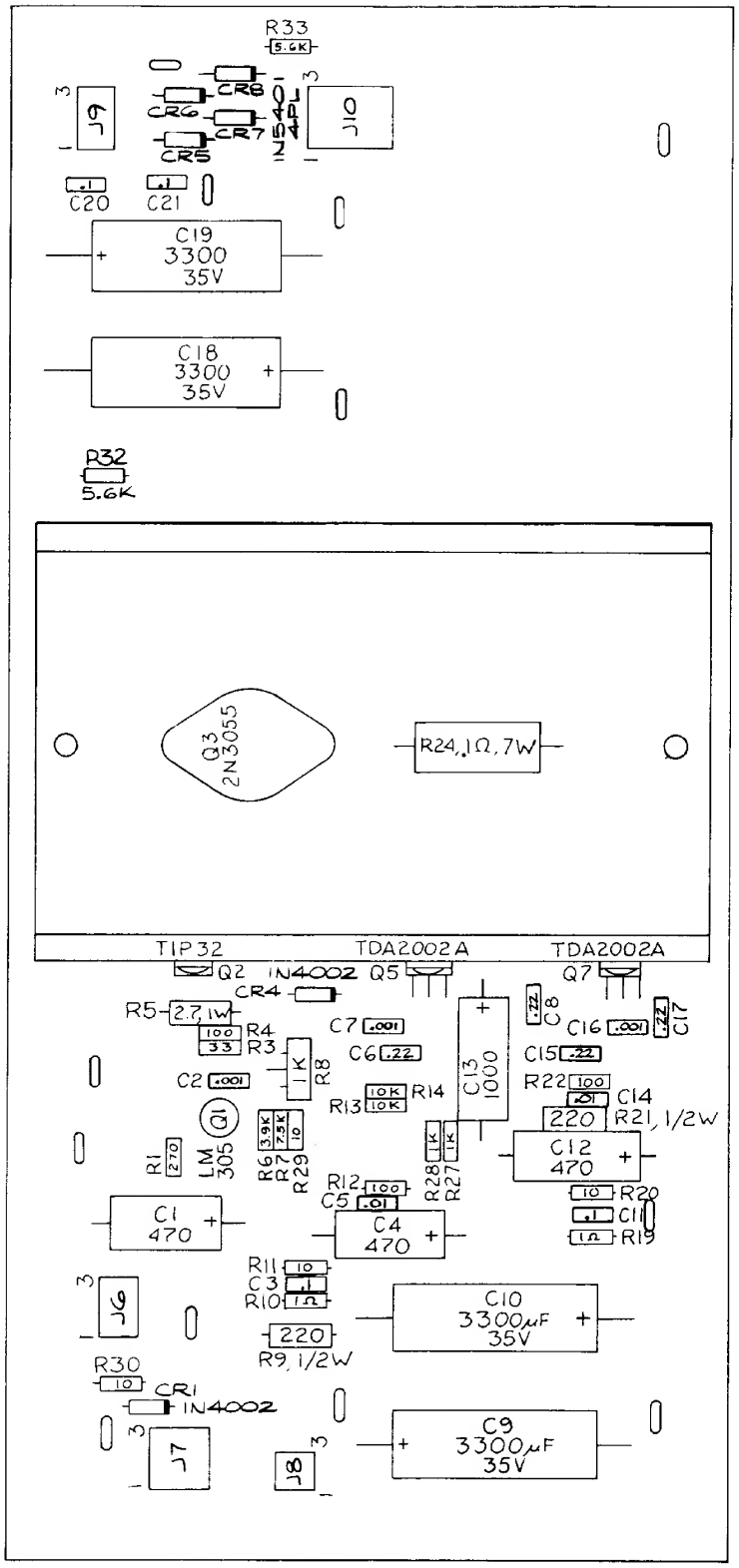


Figure 3-9 Regulator/Audio II PCB Assembly A035435-04 B

Figure 3-9 Regulator/Audio II PCB Assembly Parts List

Part No.	*Description (Reference Designations and Locations in Bold)*
19-100P1015	0.1 Ω, ±3%, 7 W Wirewound Resistor **(R24)**
19-315102	1 kΩ Vertical PCB-Mounting Cermet Trimpot **(R8)** *Acceptable substitute is part no. 119002-102*
24-250108	1000 μF, 25 V Aluminum Electrolytic Fixed Axial-Lead Capacitor **(C13)**
24-250477	470 μF, 25 V Aluminum Electrolytic Fixed Axial-Lead Capacitor **(C1, 4, 12)**
24-350338	3300 μF, 35 V Aluminum Electrolytic Fixed Axial-Lead Capacitor **(C9, 10, 18, 19)**
29-088	0.1 μF, 50 V Ceramic-Disc Axial-Lead Capacitor **(C3, 11, 20, 21)**
31-1N4002	Type-1N4002, 100 V, 1 A Silicon Rectifier Diode **(CR1, 4)**
31-1N5401	Type-1N5401, 100 V, 3 A Silicon Rectifier Diode **(CR5-8)**
33-TIP32	Type-TIP32 PNP Power Transistor **(Q2)**
34-2N3055	Type-2N3055 NPN Silicon Transistor **(Q3)**
37-LM305	5 V Linear Voltage Regulator **(Q1)**
72-1608C	#6-32 × ½-Inch Cross-Recessed Pan-Head Corrosion-Resistant Steel Machine Screw **(Q3)**
72-6606S	#6 × ⅜-Inch Cross-Recessed Pan-Head Thread-Forming Type-AB Zinc-Plated-Steel Screw **(Q5, 7)**
72-6810S	#8 x ⅝-Inch Phillips-Head Screw *(attaches PCB to cabinet wall)*
75-F60405	#6-32 × ¼-Inch Binder-Head Nylon Screw **(Q2)**
75-99516	#6-32 Nut/Washer Assembly **(Q3)**
78-16008	Thermally Conductive Compound **(Q3)**
78-16014	Thermally Conductive Silicon Insulator **(Q2)**
79-58306	6-Position Connector Receptacle **(J6, 9)**
79-58308	9-Position Connector Receptacle **(J7)**
79-58346	12-Position Connector Receptacle **(J10)**
79-58354	4-Position Connector Receptacle **(J8)**
034531-01	Heat Sink
034536-02	Foam Vibration Damper
100015-103	0.01 μF, 25 V Minimum, Ceramic-Disc Axial-Lead Capacitor **(C5, C14)** *Acceptable substitute is part no. 122005-103*
110000-010	1 Ω, ±5%, ¼ W Resistor **(R10, 19)**
110000-100	10 Ω, ±5%, ¼ W Resistor **(R11, 20, 29, 30)**
110000-101	100 Ω, ±5%, ¼ W Resistor **(R4, 12, 22)**
110000-102	1 kΩ, ±5%, ¼ W Resistor **(R27, 28)**
110000-103	10 kΩ, ±5%, ¼ W Resistor **(R13, 14)**
110000-271	270 Ω, ±5%, ¼ W Resistor **(R1)**
110000-330	33 Ω, ±5%, ¼ W Resistor **(R3)**
110000-392	3.9 kΩ, ±5%, ¼ W Resistor **(R6)**
110000-562	5.6 kΩ, ±5%, ¼ W Resistor **(R32, 33)**
110000-752	7.5 kΩ, ±5%, ¼ W Resistor **(R7)**
110001-221	220 Ω, ±5%, ½ W Resistor **(R9, 21)**
110009-027	2.7 Ω, ±5%, 1 W Resistor **(R5)**
122002-102	0.001 μF, 50 V, Ceramic-Disc Axial-Lead Capacitor **(C2, 7, 16)**
122004-224	0.22 μF, 25 V Minimum, Ceramic-Disc Axial-Lead Capacitor **(C6, 8, 15, 17)**
137151-002	Type-TDA2002A 8 W Linear Audio Amplifier Integrated Circuit **(Q5, 7)**
175004-708	#8 Spacer for Mounting Printed Circuit Board *(2 required)*
179051-002	Test Point *Acceptable substitute is part no. 020670-01*

G. Power Supply Assembly

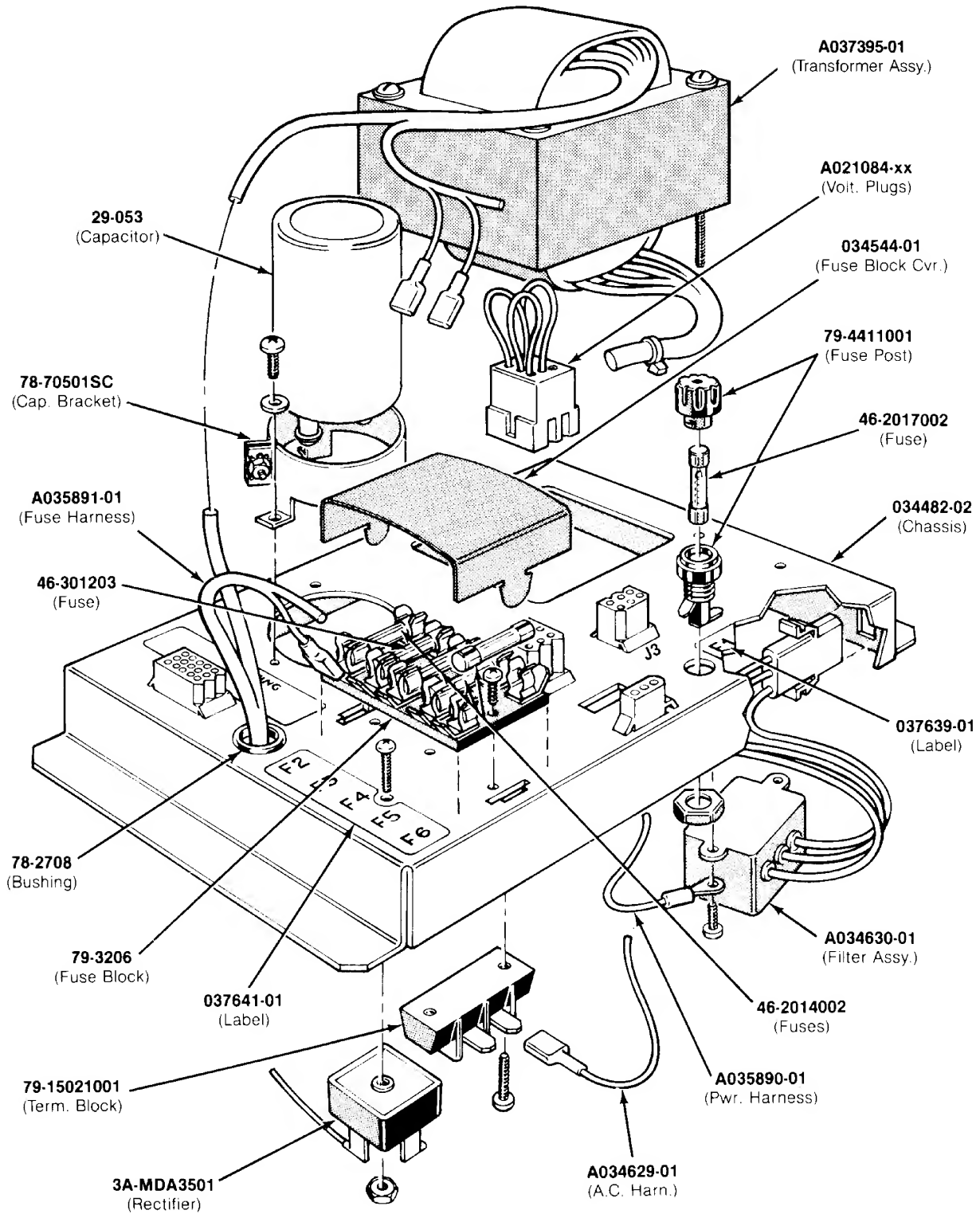


Figure 3-10 Color X-Y Power Supply Assemblies A037396-xx B

Figure 3-10 Color X-Y Power Supply Assemblies Parts List

Part No.	*Description (Reference Designations in Bold)*
A021084-01	Voltage Plug for 100 V *(violet)*
A021084-02	Voltage Plug for 120 V *(yellow)*
A021084-04	Voltage Plug for 220 V *(blue)*
A021084-05	Voltage Plug for 240 V *(brown)*
A034629-01	AC Harness Assembly
A034630-01	RFI Filter Assembly **(FL1)**
A035890-01	Power Harness Assembly
A035891-02	Fuse Harness Assembly
A037395-01	Color X-Y Transformer Assembly **(T1)**
29-053	27,000 μF 15 VDC Electrolytic Capacitor **(C1)**
3A-MDA3501	Type-MDA 3501 Bridge Rectifier **(CR1)**
46-2014002	4 A, 250 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F2, F4-F6)**
46-2017002	7 A, 250 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F1)**
46-301203	20 A, 32 V, 3AG Slow-Blow Glass Cartridge-Type Fuse **(F3)**
78-2708	Nylon Type 6/6 Hole Bushing with ⅝-Inch Inside Diameter × 5/64-Inch Outside Diameter × ¼-Inch Thick
78-70501SC	2-Inch Diameter Capacitor Mounting Bracket
79-15021001	2-Circuit Single-Row Terminal Block
79-3206	5-Position 3AG Fuse Block with ¼-Inch Quick-Disconnect Terminals
79-4411001	Panel-Mounting Non-Indicating 3AG Cartridge-Type Fuse Post
034482-02	Power Supply Chassis Base
034544-01	Fuse Block Cover
037243-01	Metal Base Plate *(not shown in illustration)*
037639-01	Label for Fuse Value **(F1)**
037641-01	Label for Fuse Values **(F2-F6)**

NOTE

A037396-01 power supply assembly has the 120 V plug
A037396-02 has the 100 V, 220 V, and 240 V plugs
A037396-03 has the 220 V and 240 V plugs

Line Voltage Range	**Voltage Selection Plug Wire Color**
90-110 VAC (100)	**Violet**
105-135 VAC (120)	**Yellow**
200-240 VAC (220)	**Blue**
220-260 VAC (240)	**Brown**

WARNING

Fuse cover must be in place during game operation.

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NOTE

This staple temporarily holds the schematic package together. Remove the staple before using the schematics.

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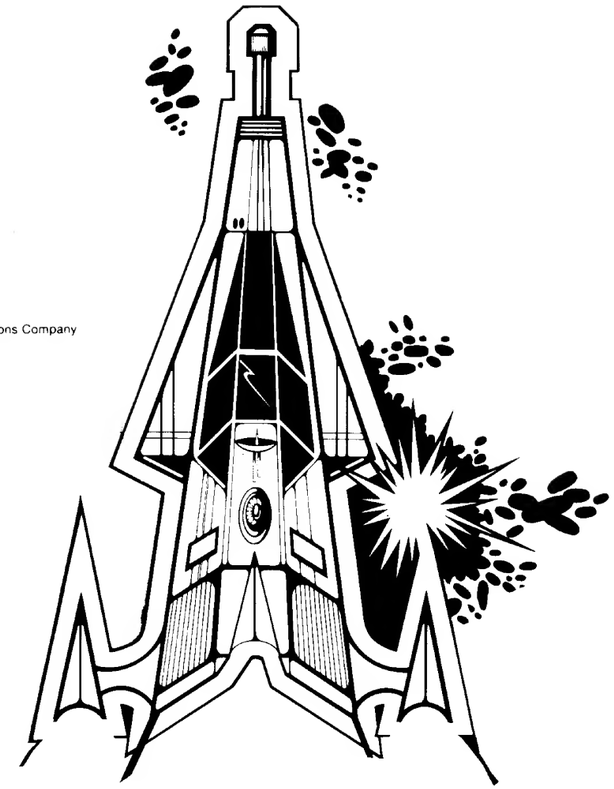
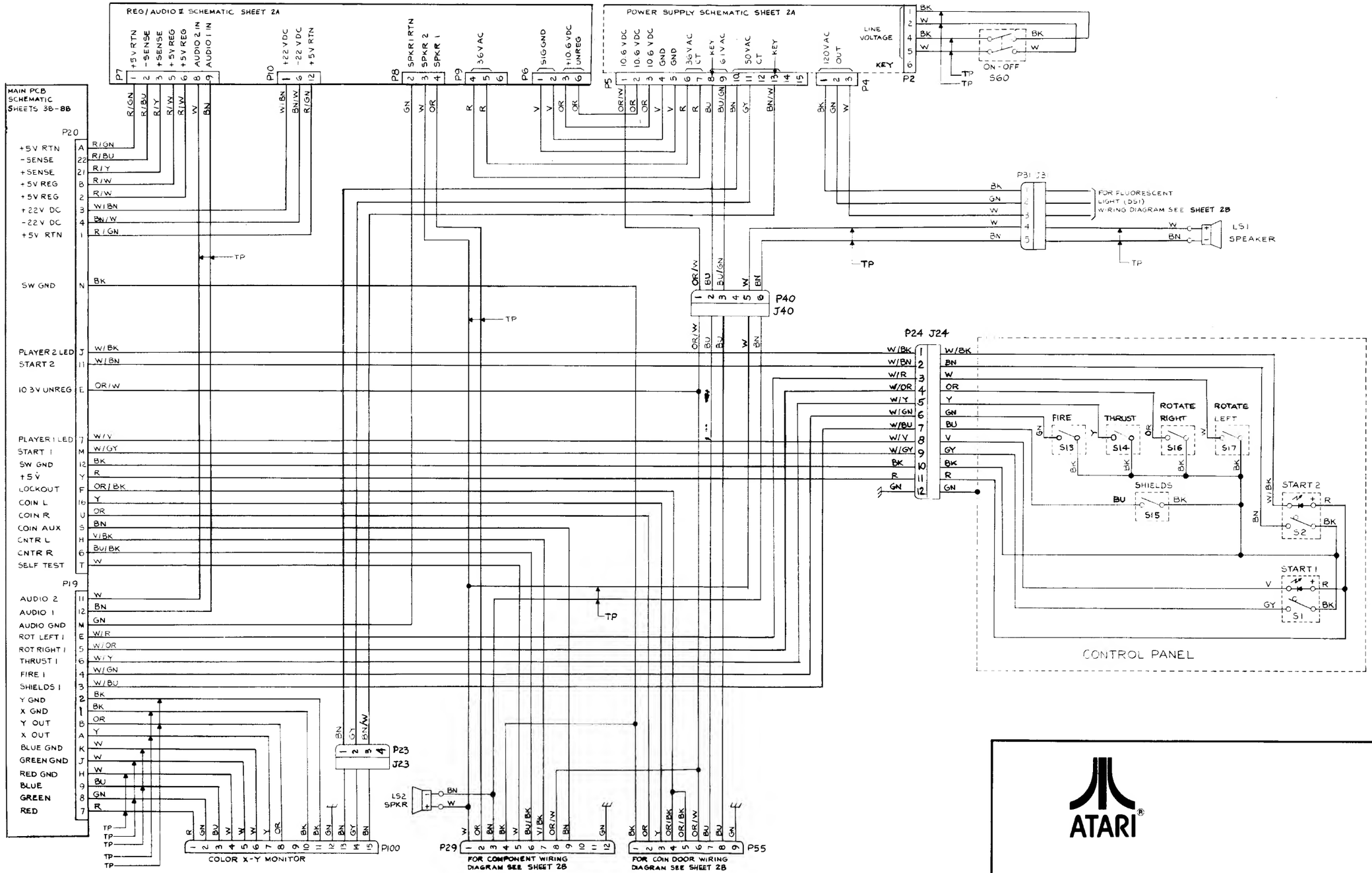


Schematic Package Supplement to

Operation, Maintenance and Service Manual

7L

SP-206 Sheet 1A
1st printing



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Gravitar Main Wiring Diagram

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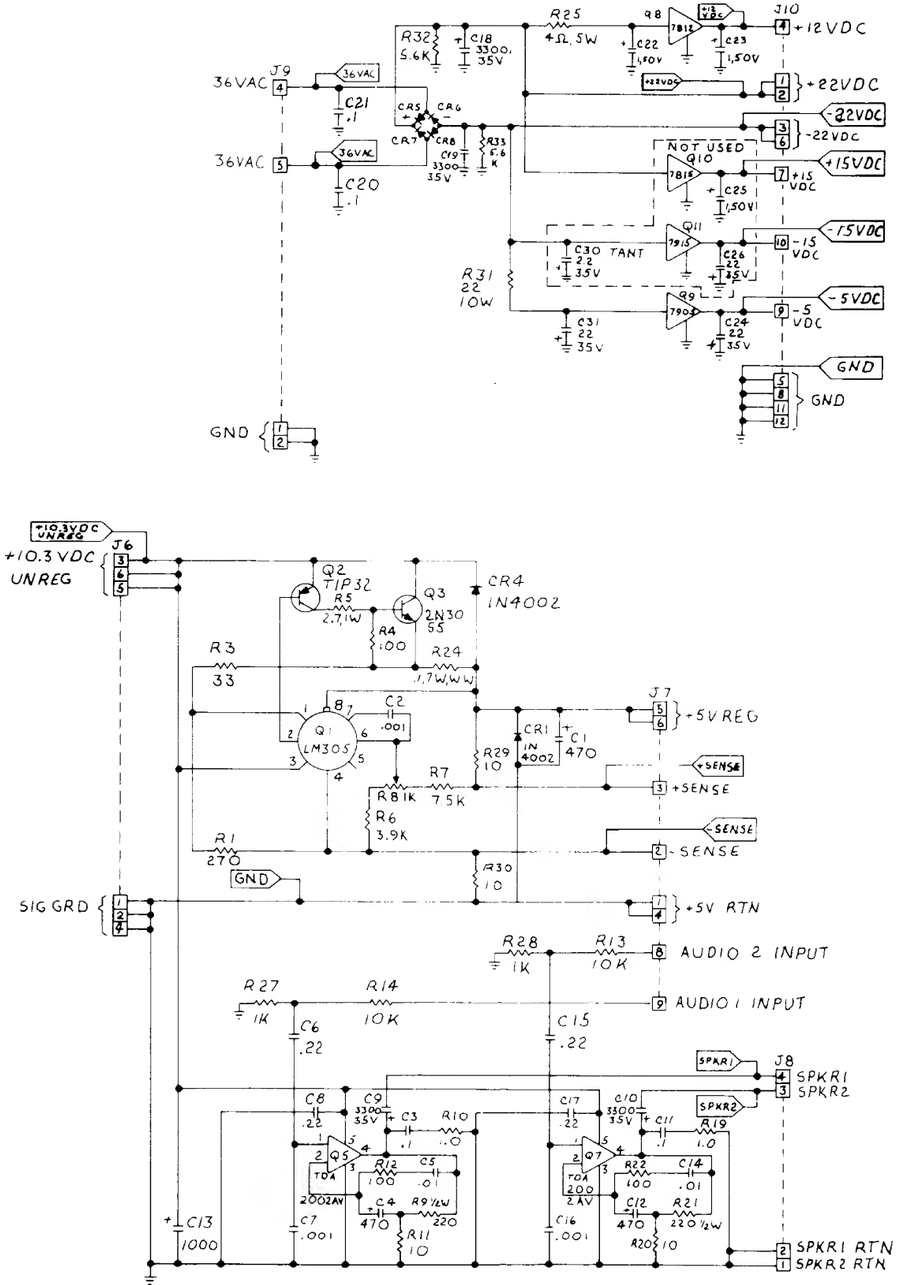
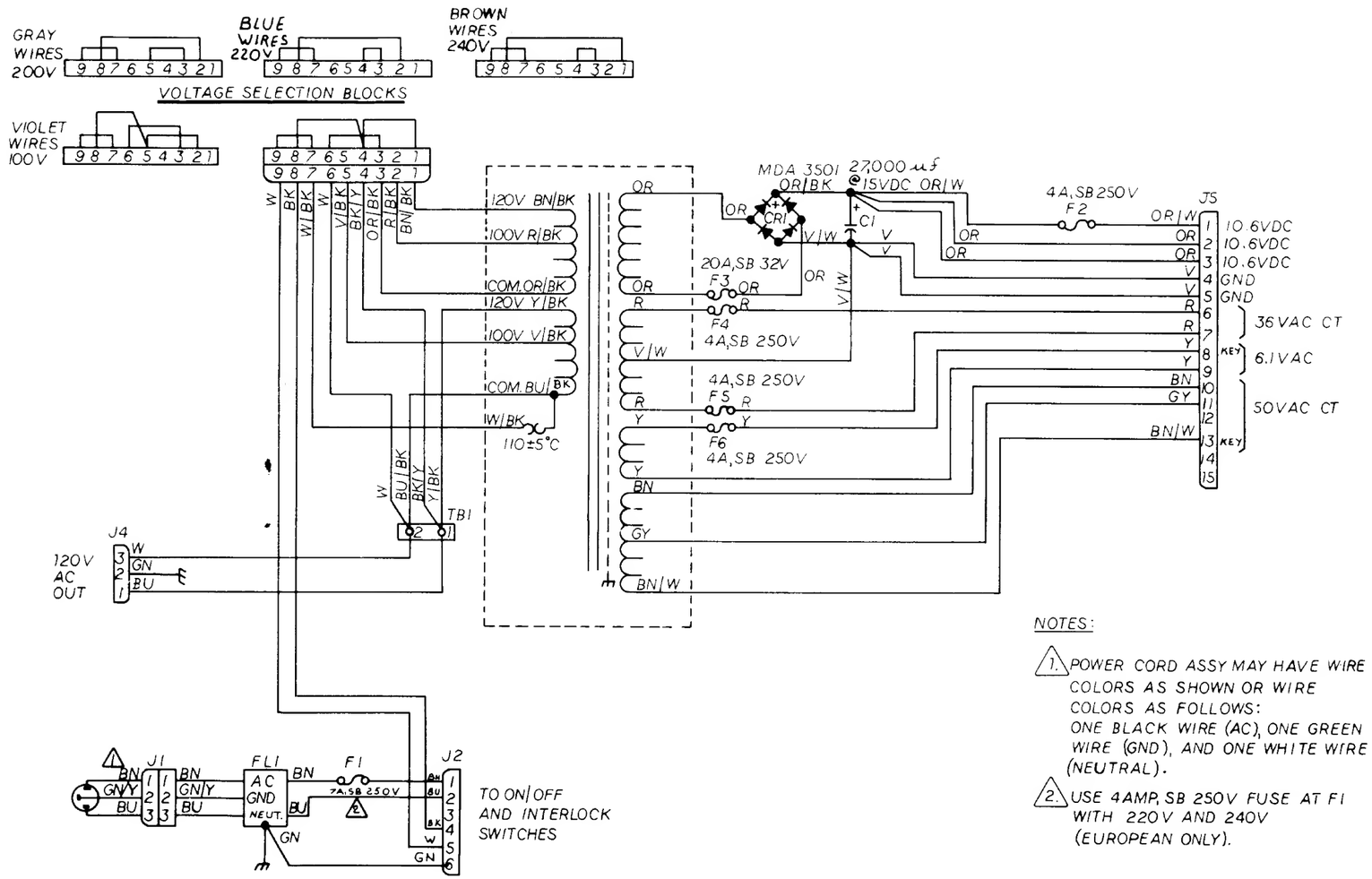
Regulator/Audio II PCB Schematic Diagram



COLOR X-Y POWER SUPPLY DIAGRAM



NOTES:

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND), AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V AND 240V (EUROPEAN ONLY).

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Gravitar™ Power Supply and Reg./Audio II PCB

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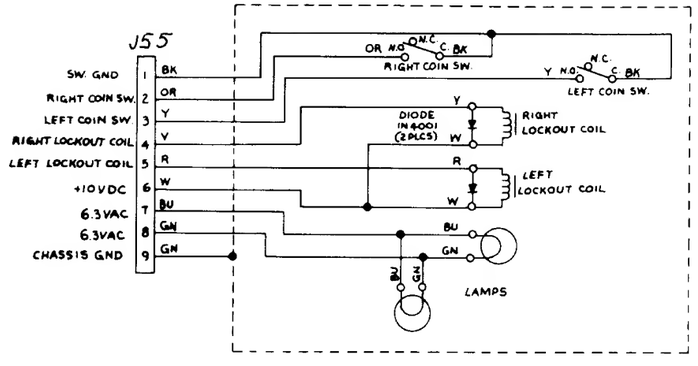
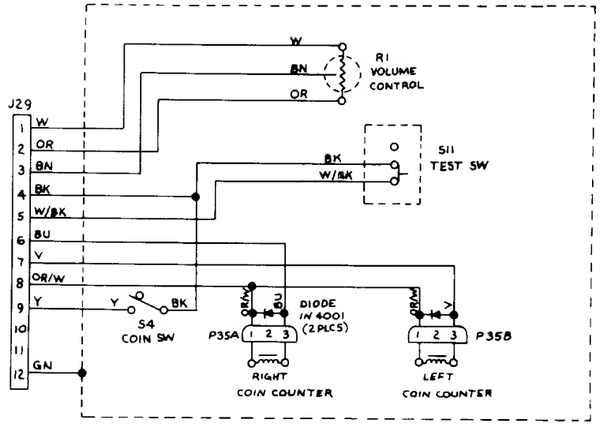
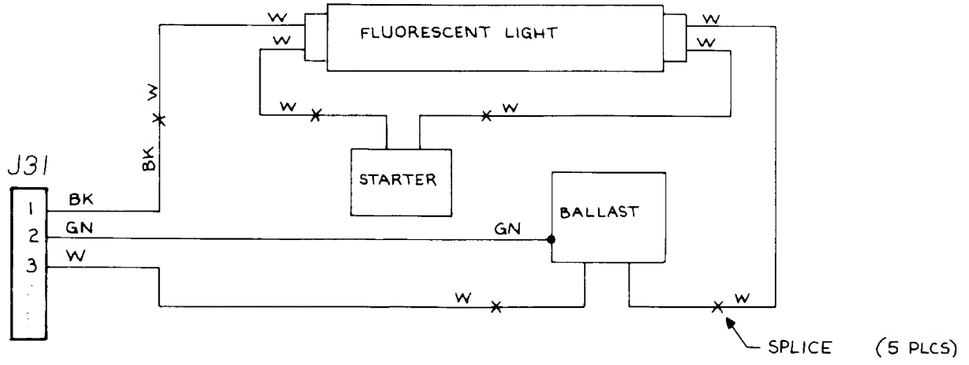
Coin Door Wiring Diagram



Utility Panel Wiring Diagram



Fluorescent Light and Speaker Wiring Diagram



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Gravitar™ Game Wiring Interfaces

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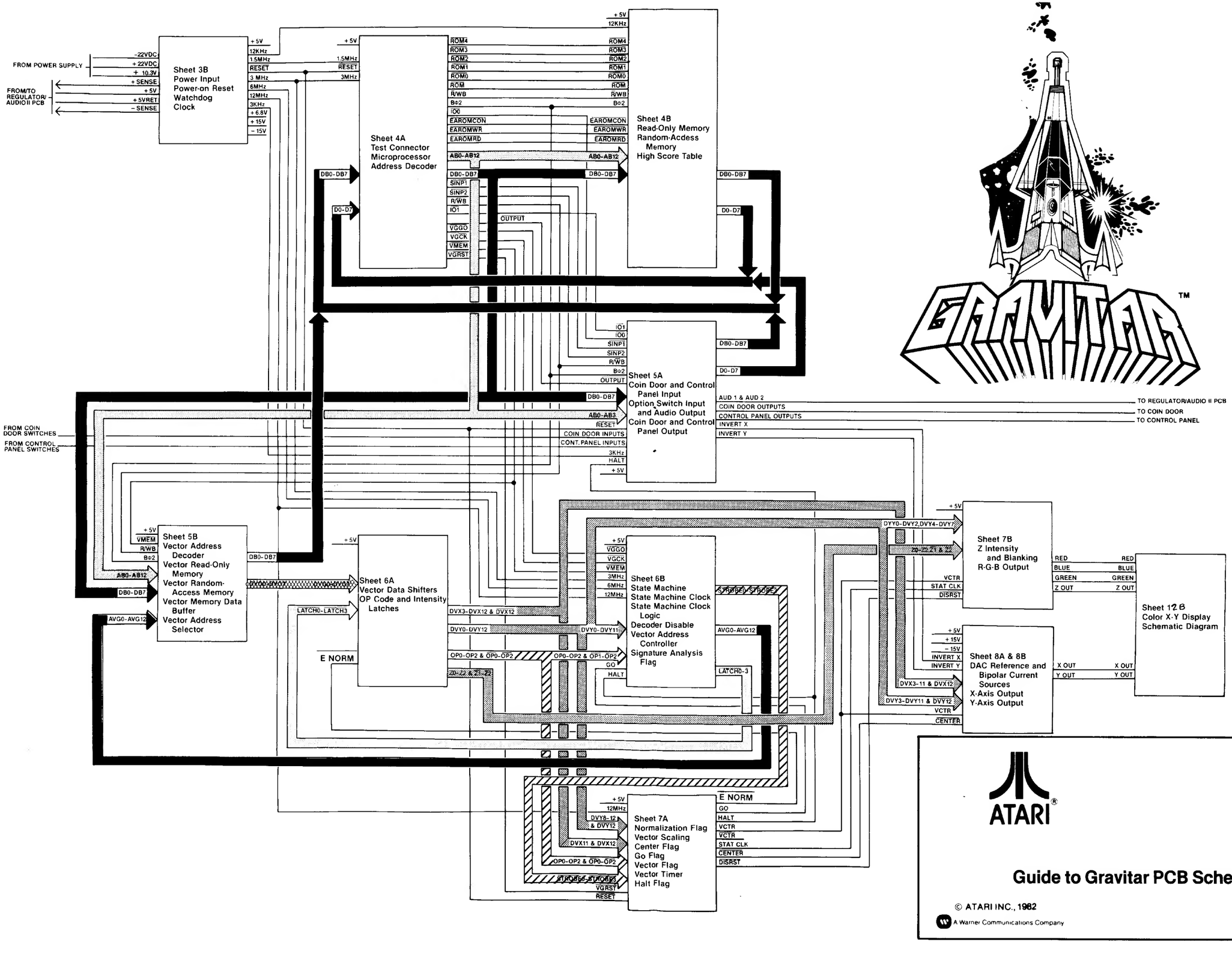
FROM POWER SUPPLY
-22VDC
+22VDC
+10.3V
+SENSE
FROM/TO REGULATOR/ AUDIO II PCB
+5V
+5VRET
-SENSE
Sheet 3B
Power Input
Power-on Reset
Watchdog
Clock
+5V
12KHz
1.5MHz
RESET
3 MHz
6MHz
12MHz
3KHz
+6.8V
+15V
-15V
Sheet 4A
Test Connector
Microprocessor
Address Decoder
ROM4
ROM3
ROM2
ROM1
ROM0
ROM
R/WB
B∅2
IO0
EAROMCON
EAROMWR
EAROMRD
AB0-AB12
DB0-DB7
SINP1
SINP2
IO1
VGGO
VGCK
VMEM
VGRST
D0-D7
OUTPUT
Sheet 4B
Read-Only Memory
Random-Acdess
Memory
High Score Table
Sheet 5A
Coin Door and Control
Panel Input
Option Switch Input
and Audio Output
Coin Door and Control
Panel Output
AB0-AB3
RESET
COIN DOOR INPUTS
CONT. PANEL INPUTS
HALT
AUD 1 & AUD 2
COIN DOOR OUTPUTS
CONTROL PANEL OUTPUTS
INVERT X
INVERT Y
TO REGULATOR/AUDIO II PCB
TO COIN DOOR
TO CONTROL PANEL
FROM COIN DOOR SWITCHES
FROM CONTROL PANEL SWITCHES
Sheet 5B
Vector Address
Decoder
Vector Read-Only
Memory
Vector Random-
Access Memory
Vector Memory Data
Buffer
Vector Address
Selector
Sheet 6A
Vector Data Shifters
OP Code and Intensity
Latches
LATCH0-LATCH3
E NORM
DVX3-DVX12 & DVX12
DVY0-DVY12
DVY0-DVY11
OP0-OP2 & OP0-OP2
OP0-OP2 & OP1-OP2
Z0-Z2 & Z3-Z3
Sheet 6B
State Machine
State Machine Clock
State Machine Clock
Logic
Decoder Disable
Vector Address
Controller
Signature Analysis
Flag
GO
HALT
STROBE0-STROBE2
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LATCH0-3
Sheet 7A
Normalization Flag
Vector Scaling
Center Flag
Go Flag
Vector Flag
Vector Timer
Halt Flag
DVY8-12 & DVY12
DVX11 & DVX12
VGRST
RESET
VCTR
STAT CLK
CENTER
DISRST
DVY0-DVY2,DVY4-DVY7
Z0-Z2 & Z3
Sheet 7B
Z Intensity
and Blanking
R-G-B Output
RED
BLUE
GREEN
Z OUT
Sheet 8A & 8B
DAC Reference and
Bipolar Current
Sources
X-Axis Output
Y-Axis Output
X OUT
Y OUT
DVX3-11 & DVX12
DVY3-DVY11 & DVY12
Sheet 12 B
Color X-Y Display
Schematic Diagram
GRAVITAR
TM
ATARI
Guide to Gravitar PCB Schematics
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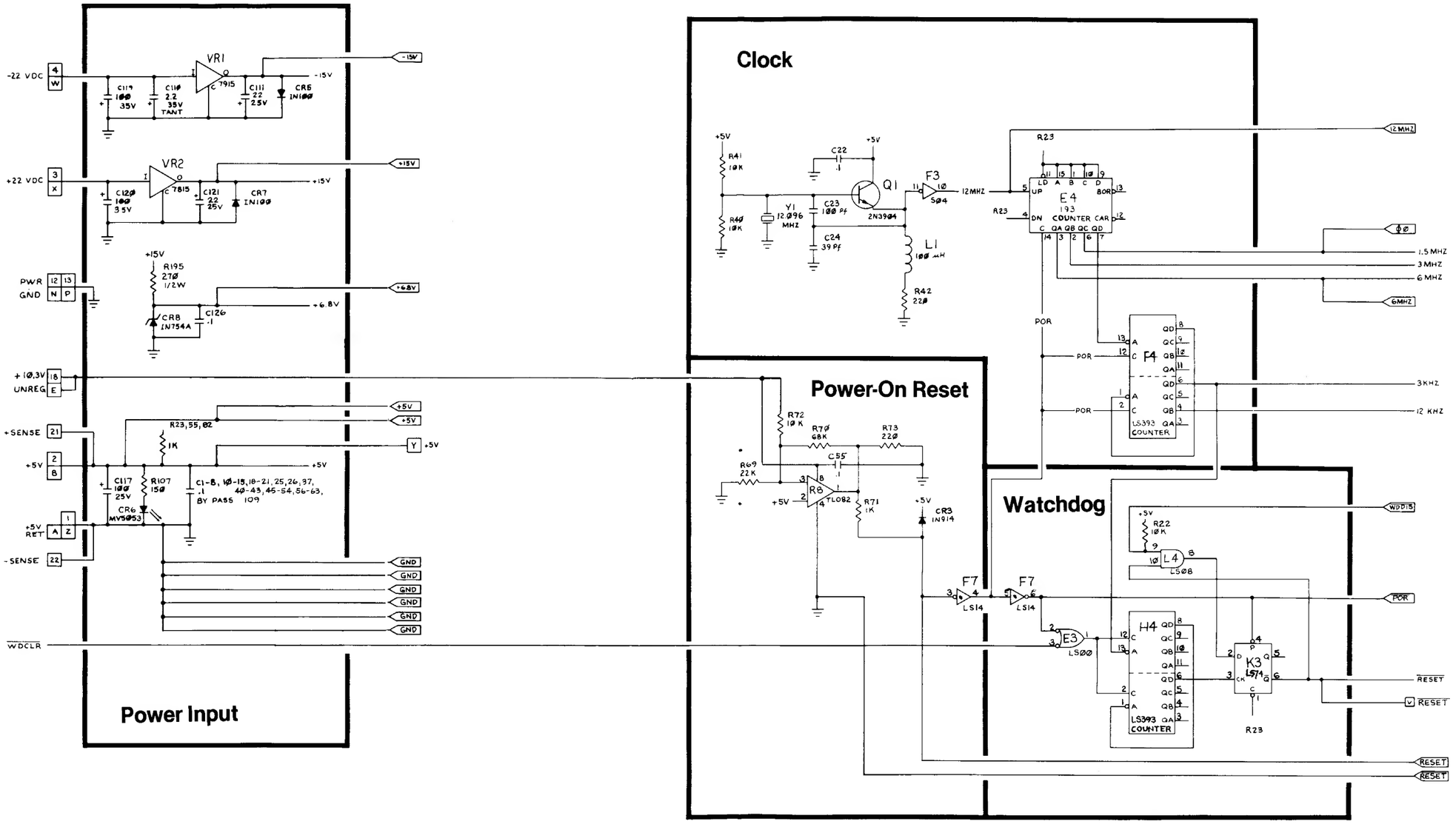
1st printing



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Gravitar™ PCB Schematic Diagram

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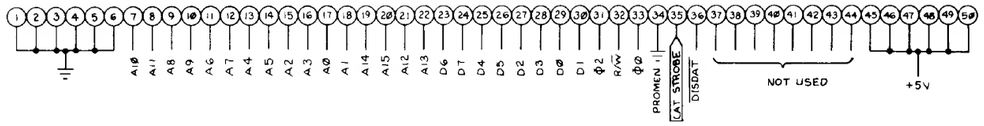
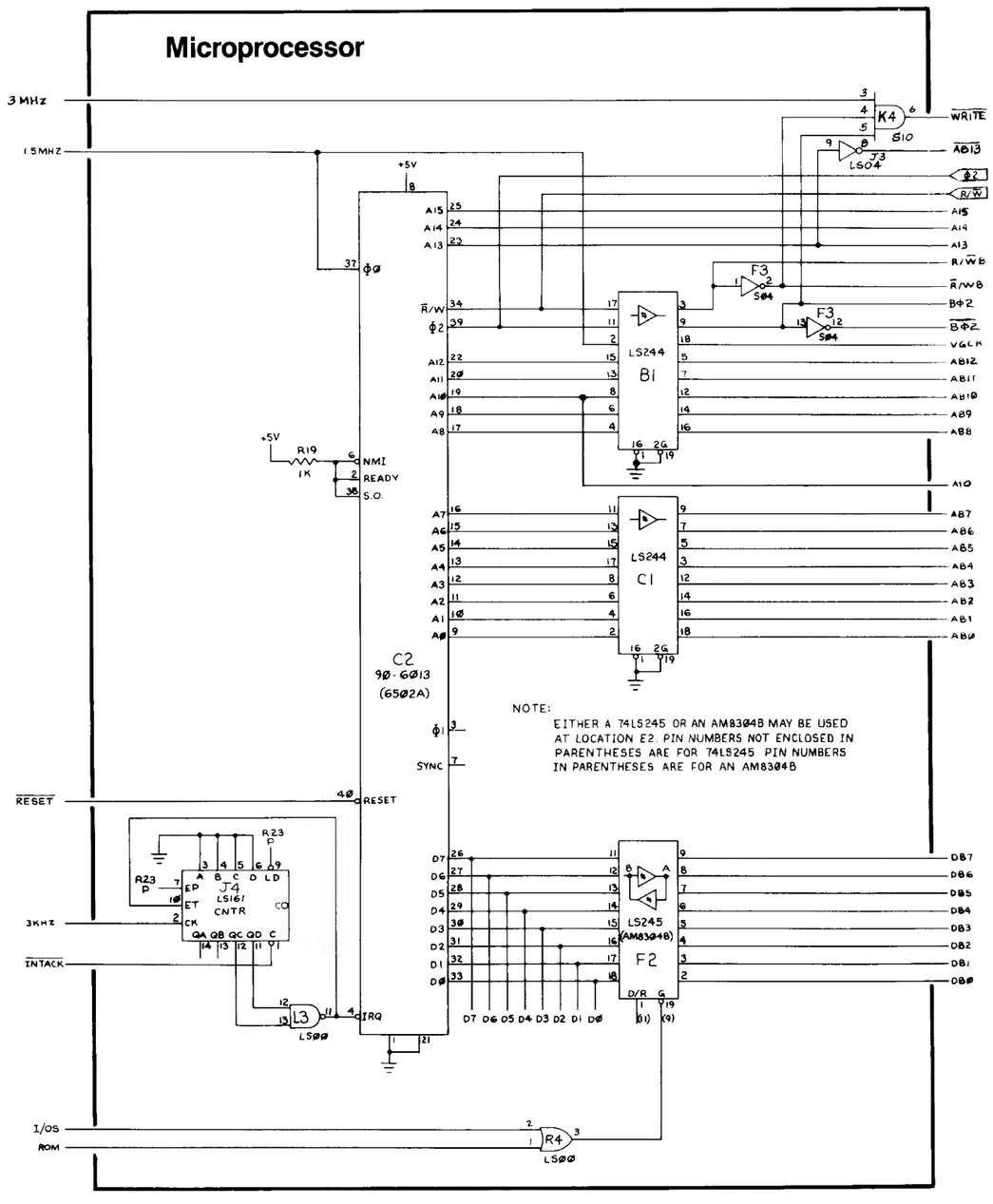
Test Connector

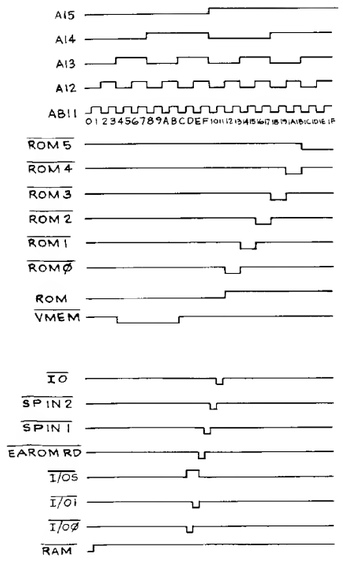


Microprocessor

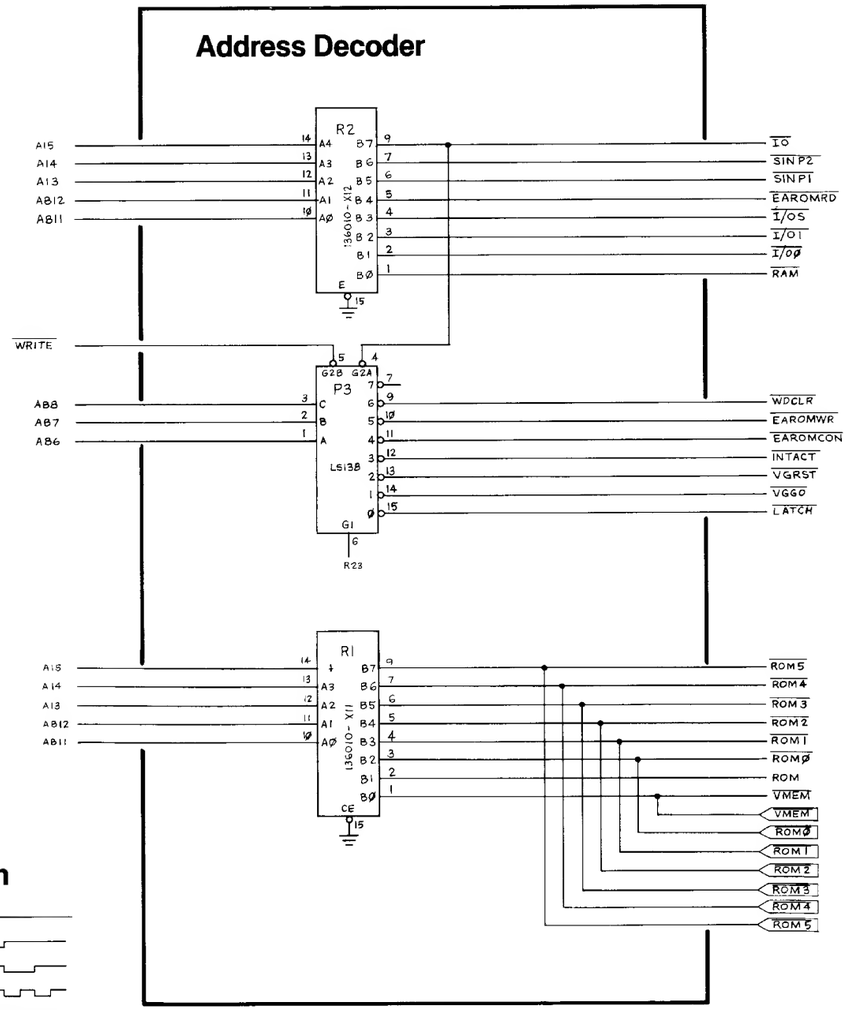


NOTE:
EITHER A 74LS245 OR AN AM8304B MAY BE USED AT LOCATION E2. PIN NUMBERS NOT ENCLOSED IN PARENTHESES ARE FOR 74LS245. PIN NUMBERS IN PARENTHESES ARE FOR AN AM8304B.

Timing Diagram



Address Decoder



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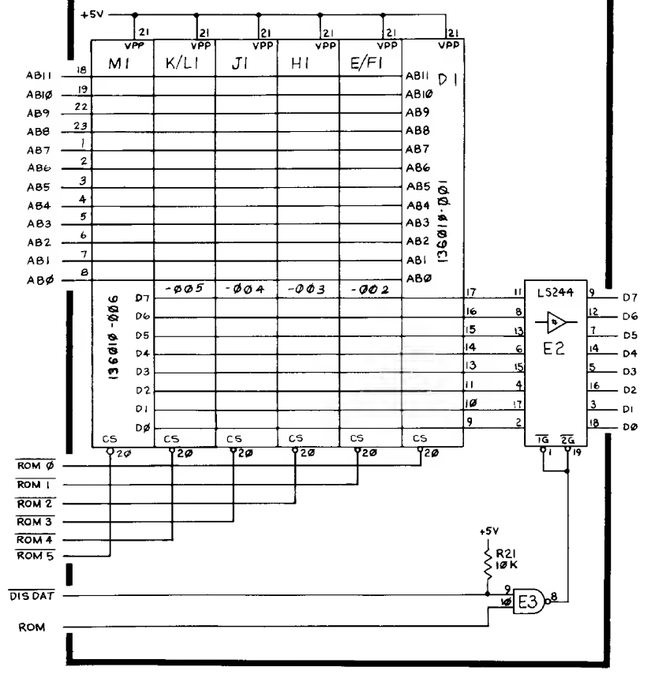
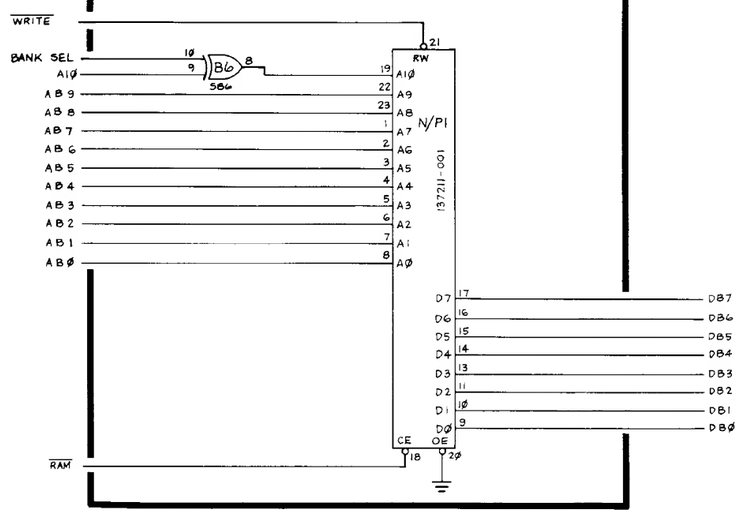
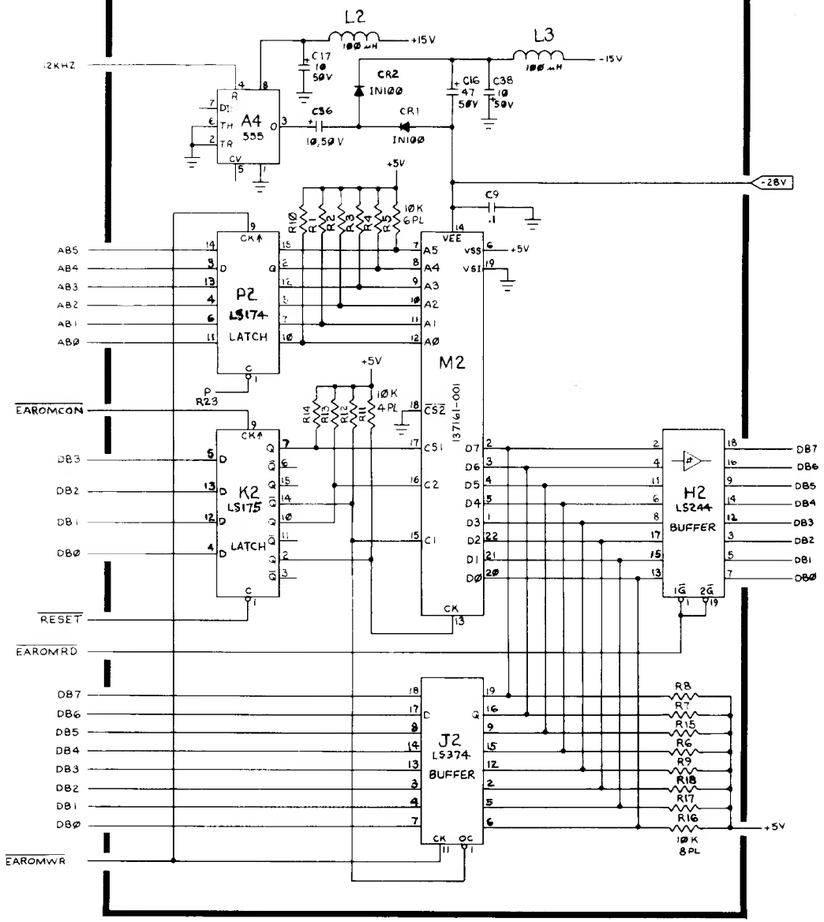
Read-Only Memory



Random-Access Memory



High-Score Table



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Gravitar™ PCB Schematic Diagram

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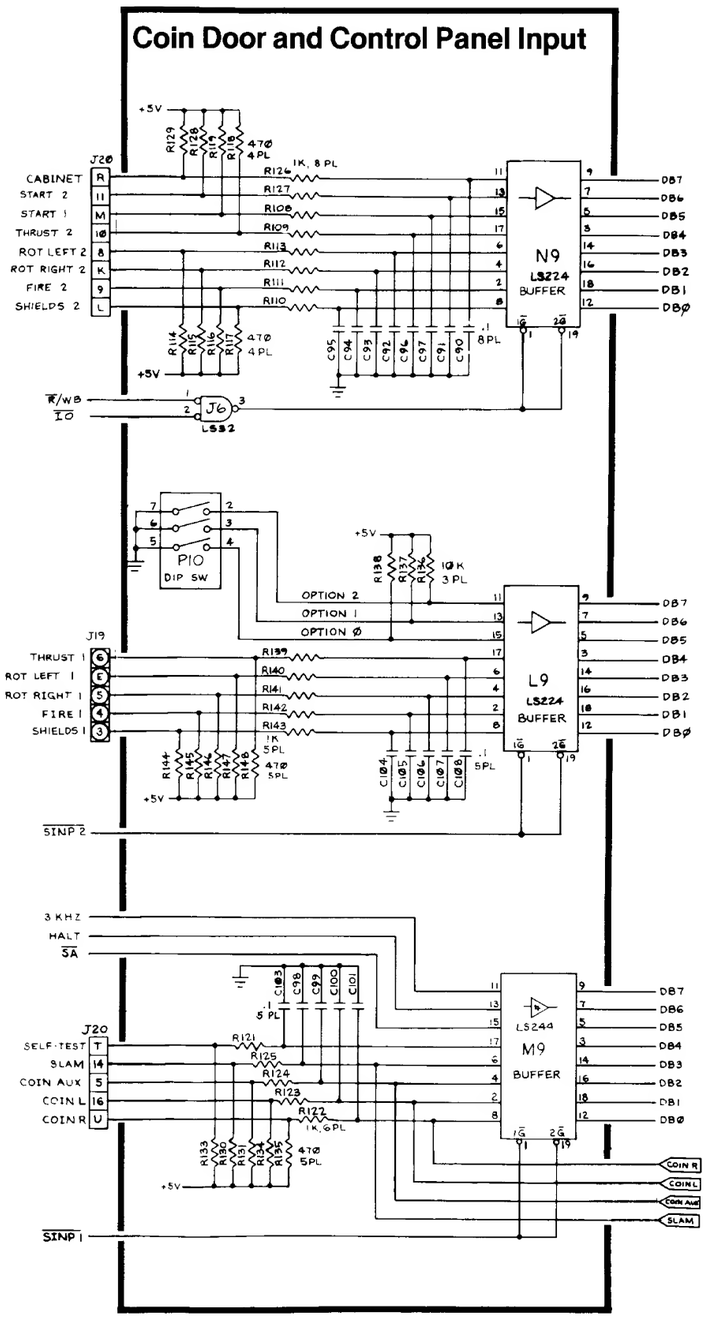
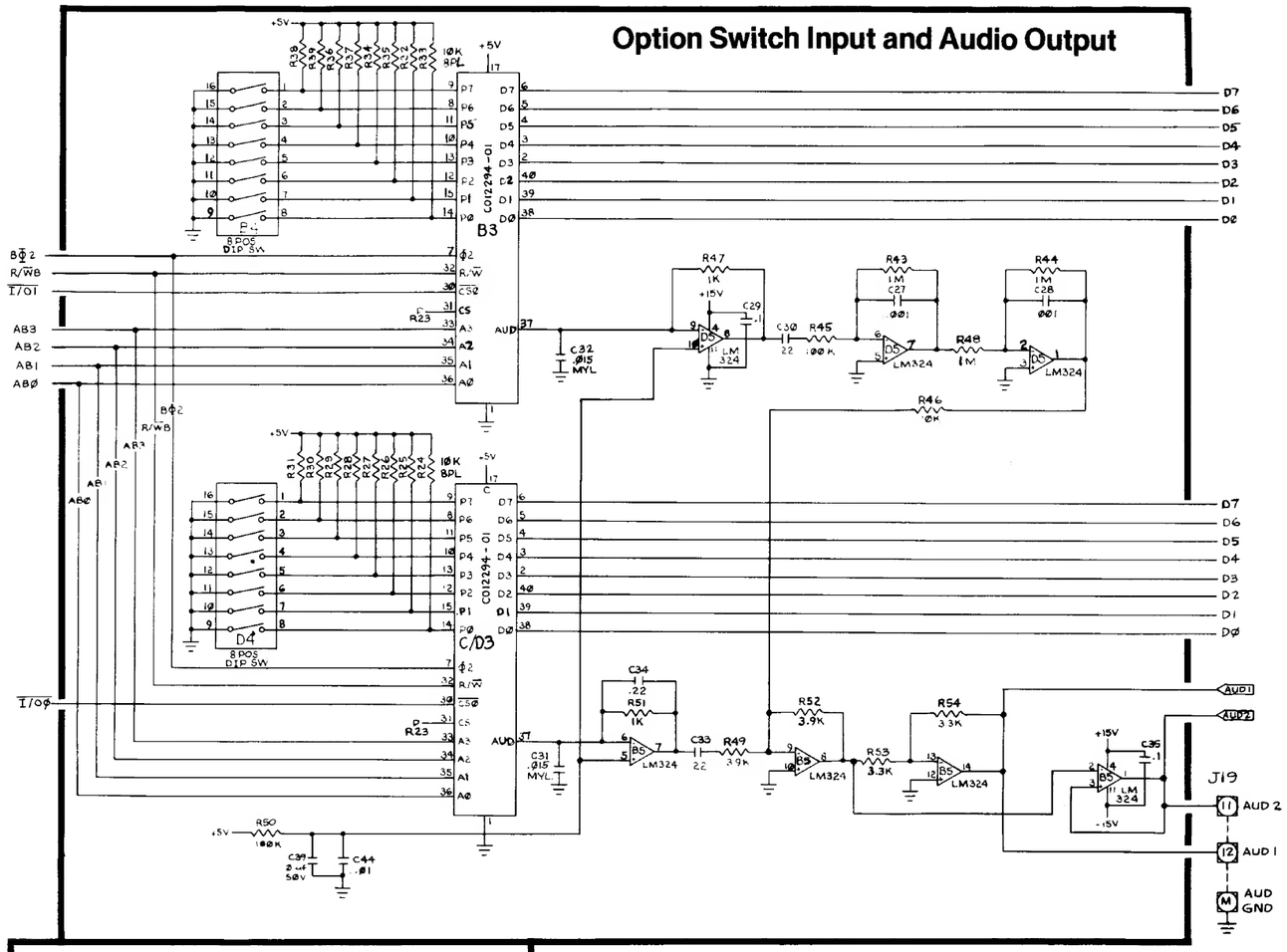
1st printing

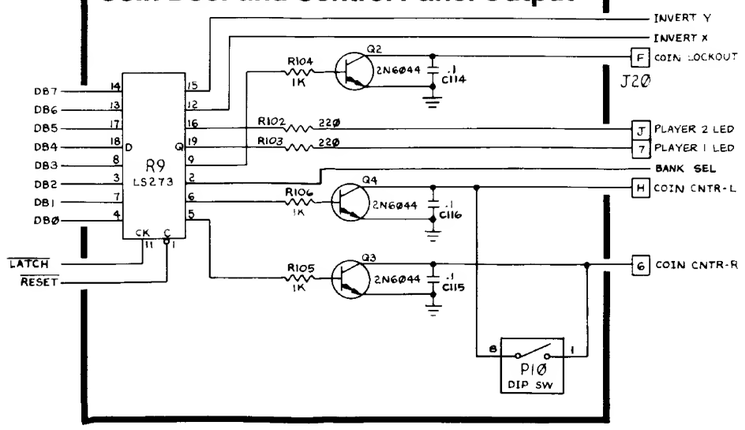
Coin Door and Control Panel Input



Option Switch Input and Audio Output



Coin Door and Control Panel Output



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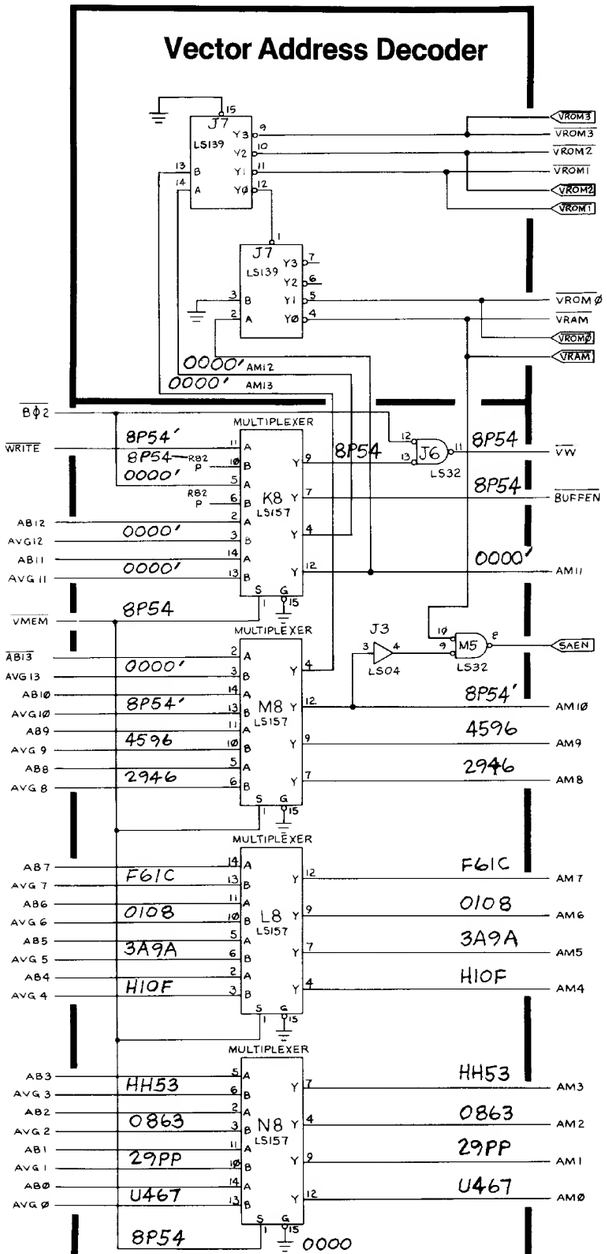
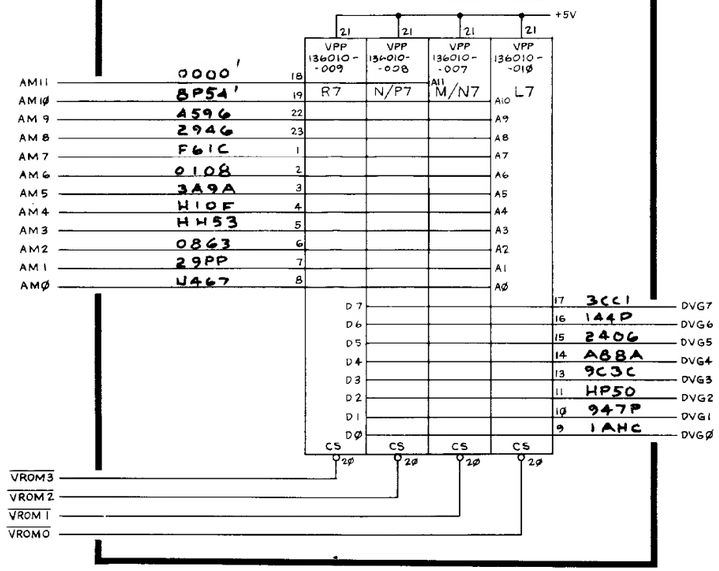
Vector Address Decoder

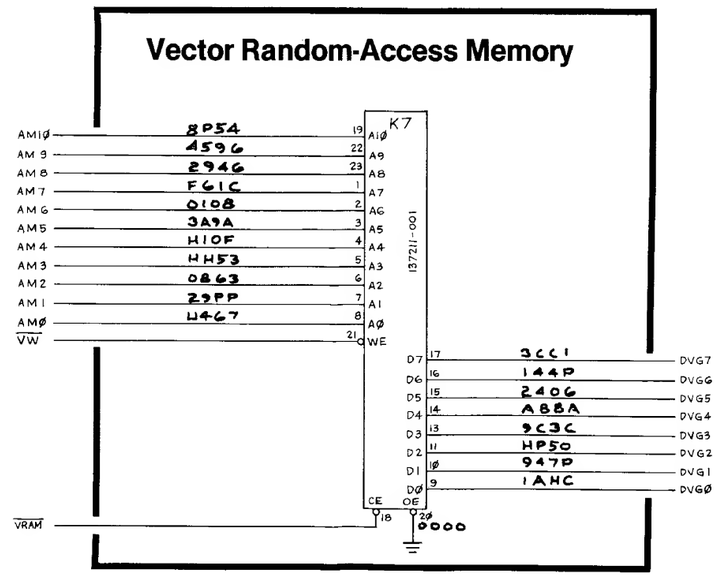


Vector Address Selector

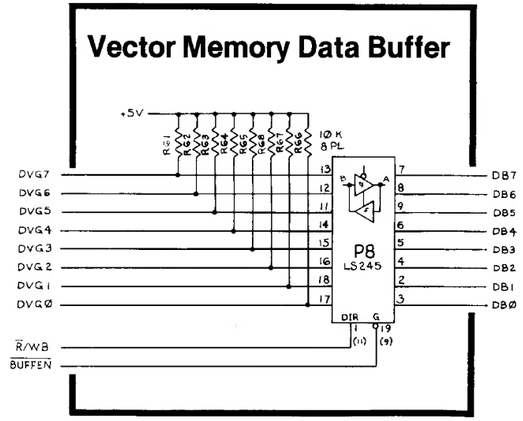
Vector Read-Only Memory



Vector Random-Access Memory



Vector Memory Data Buffer



NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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Gravitar™ PCB Schematic Diagram

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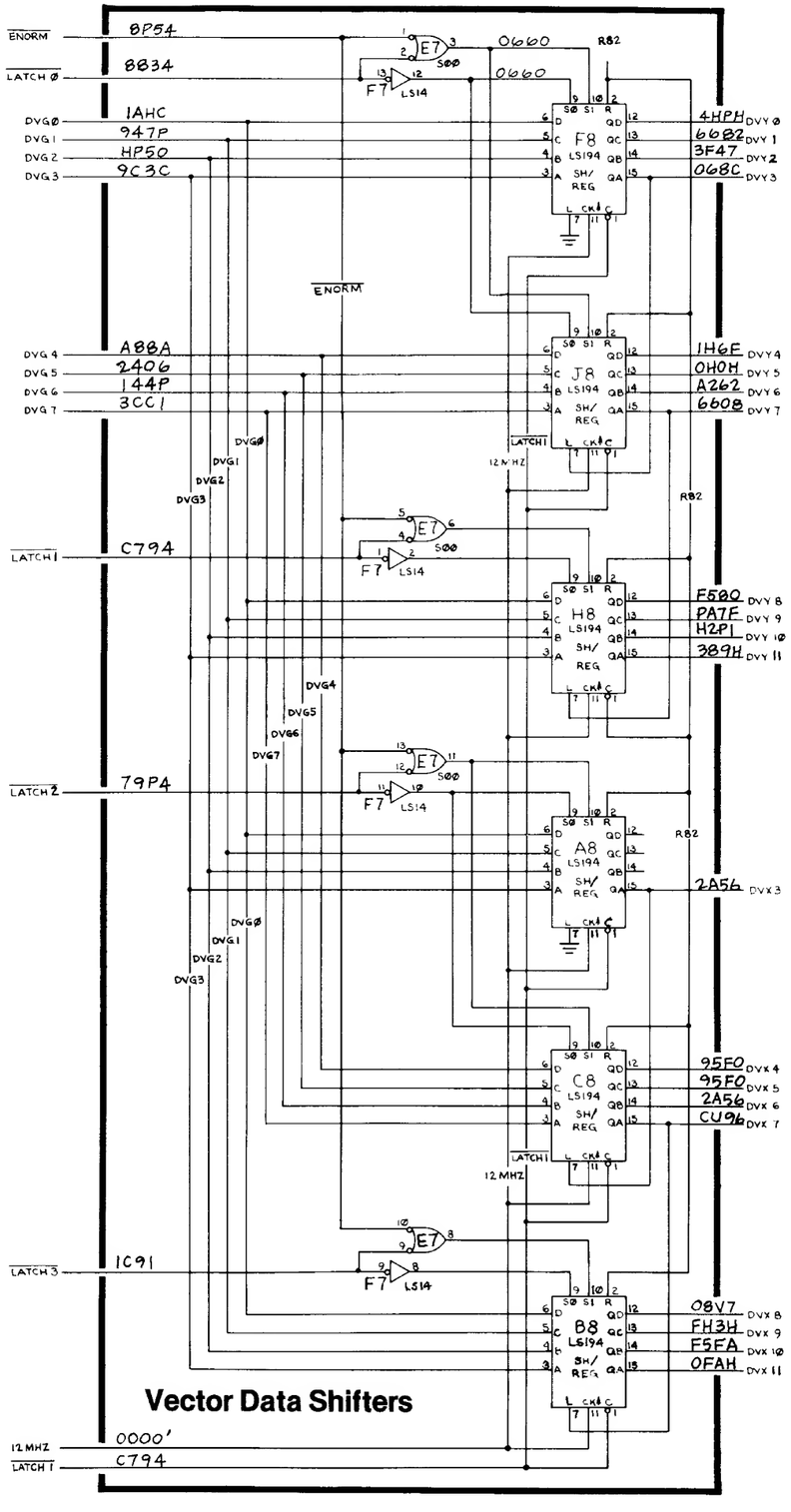
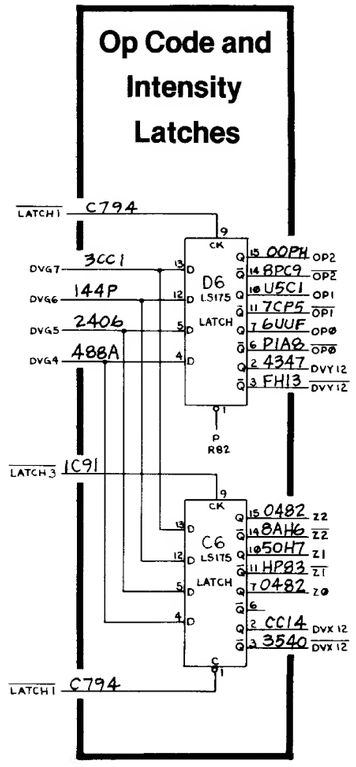
1st printing





NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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Gravitar™ PCB Schematic Diagram

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State Machine Clock

State Machine Clock Logic

Decoder Disable

Signature Analysis Flag

Address Controller

State Machine

NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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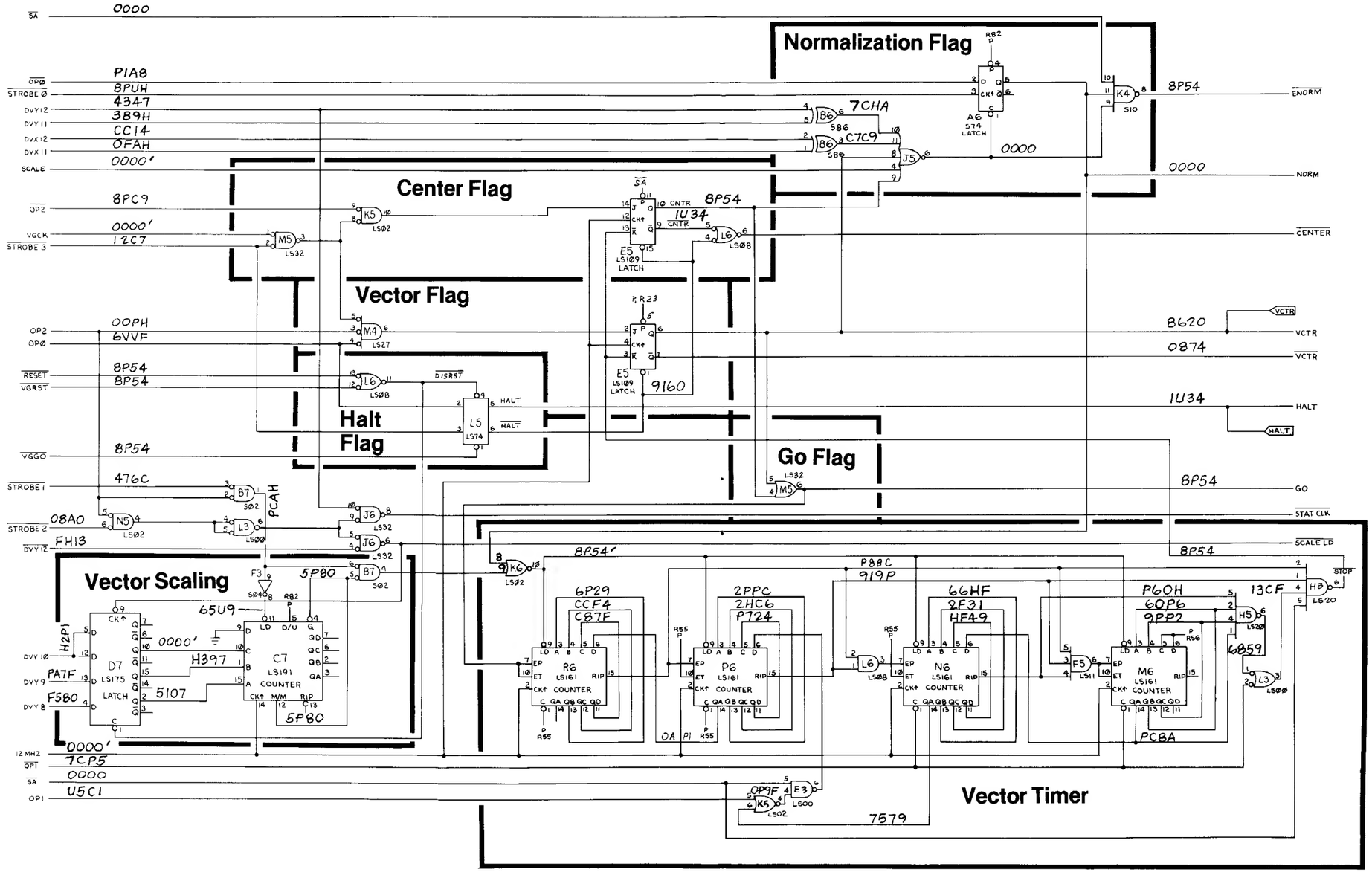

NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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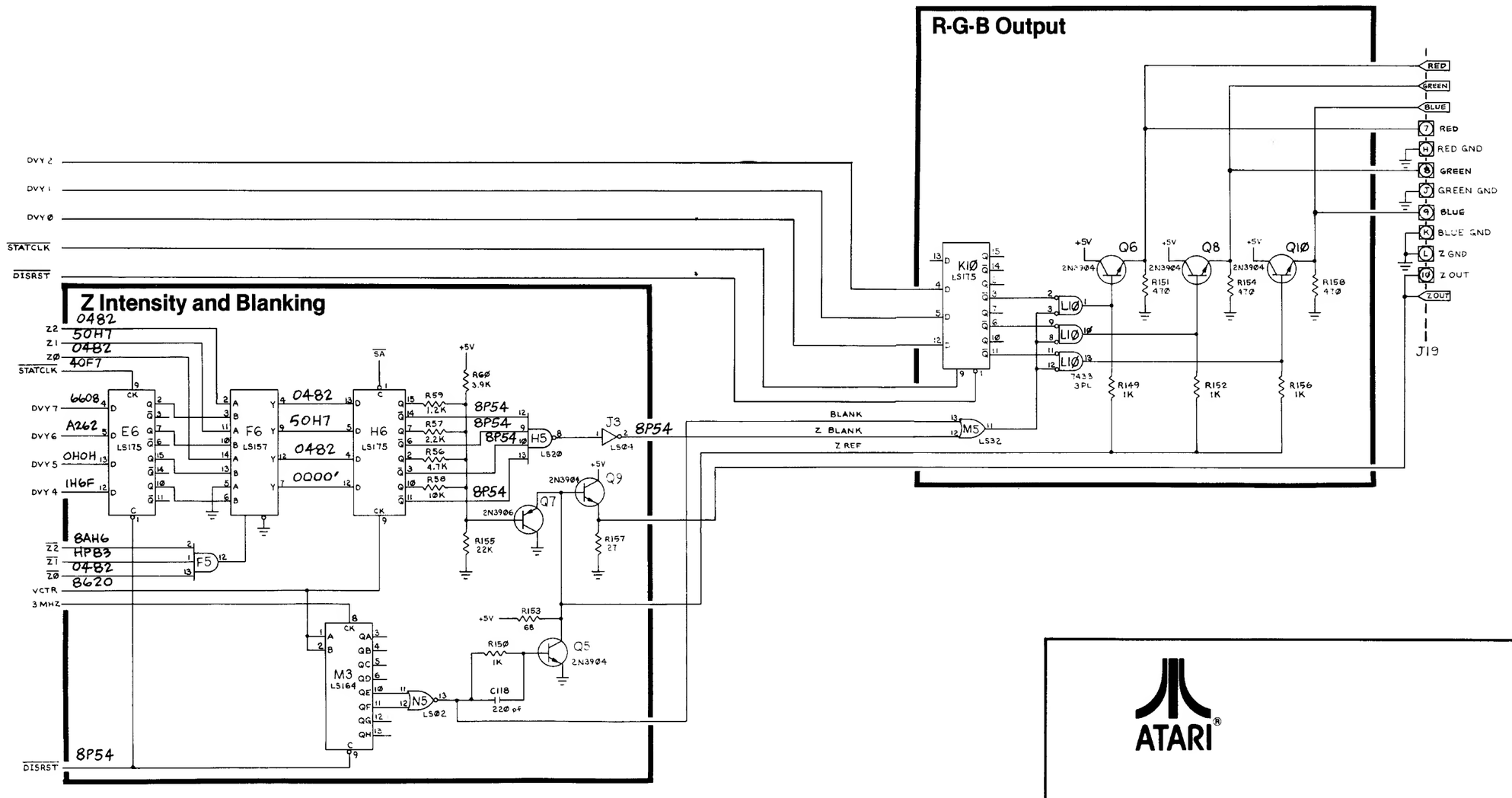
NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.



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Gravitar™ PCB Schematic Diagram

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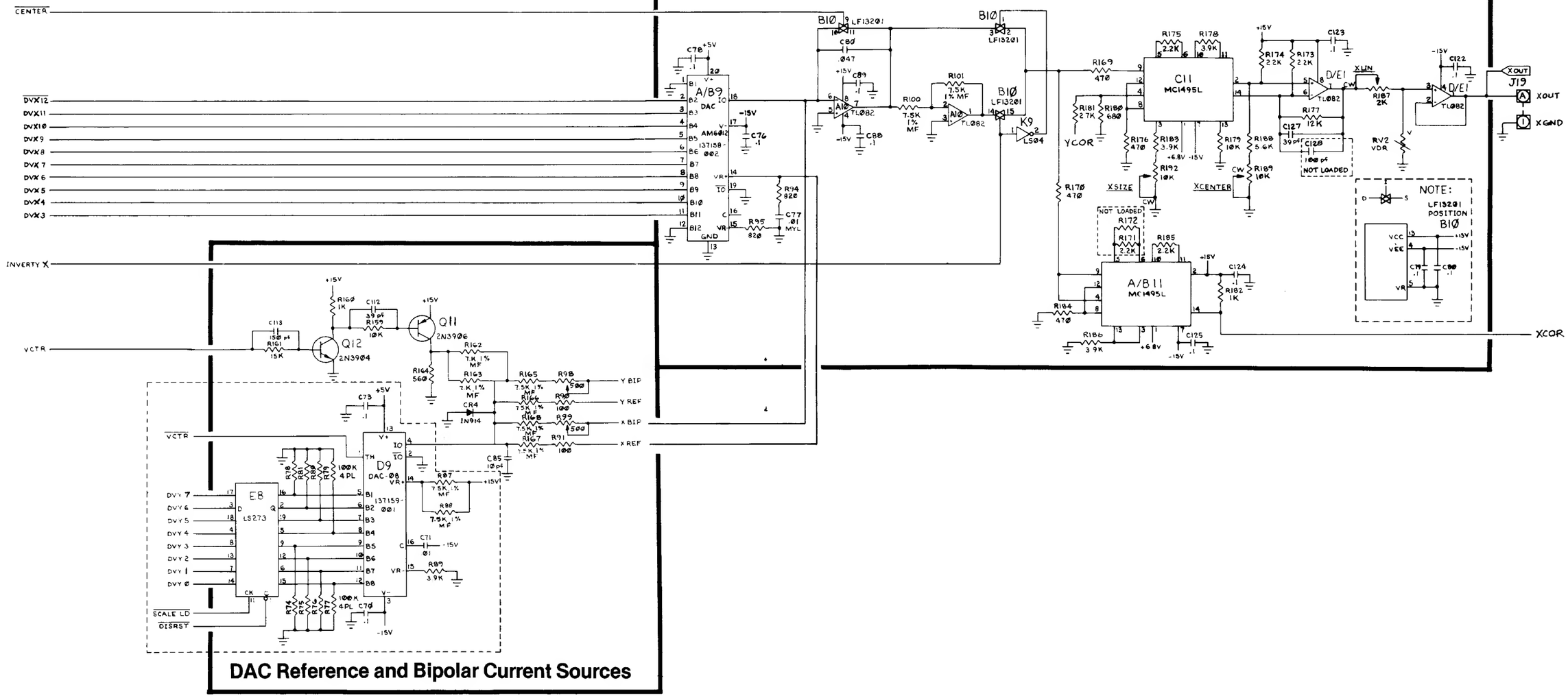
X-Axis Output



DAC Reference and Bipolar Current Sources

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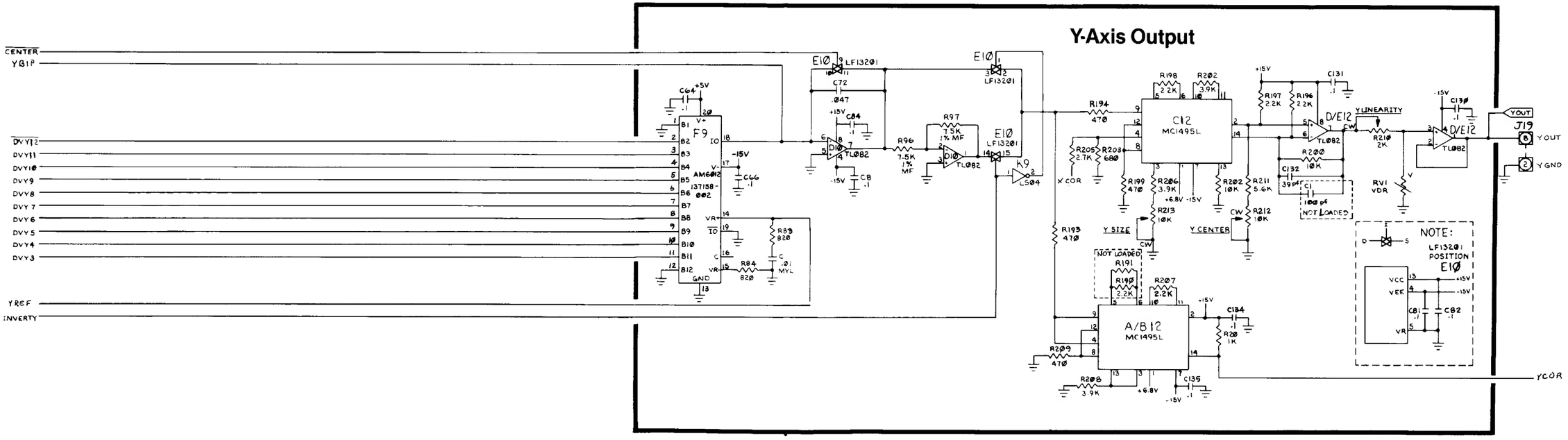

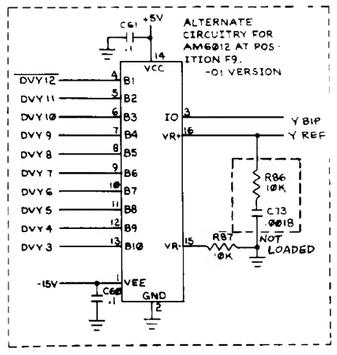

Adjusting X- and Y-Axis Video Potentiometers

If you replace the main Gravitar PCB or the display, you may have to make the following adjustments:

1. Enter self-test and advance to diagonal crosshatch pattern (Screen 2).
2. *Centering Pots:* Adjust X CENTER (R189) and Y CENTER (R212) so that the crosshatch pattern is located at the middle of the screen.
3. *Size Pots:* Adjust XSIZE (R192) and YSIZE (R213) so that the crosshatch pattern exactly covers the whole visible screen.
4. *Linearity Pots:* Adjust XLIN (R187) and YLIN (R210) so that the diagonal lines are straight. Since the LIN pots change the size of the displayed picture on the screen, you may have to readjust the SIZE pots in order to get the correct adjustment.
5. *Bipolar Pots:* Advance to the self-test raster pattern (Screen 4). Adjust XBIP (R99) and YBIP (R98) for a 1-inch high horizontal raster in the center of the screen. Be sure the raster ends are square with the sides of the outer rectangle.

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Gravitar™ PCB Schematic Diagram

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Descriptions of Gravitar PCB Signal Names

A10, A13-A15

Address bits on Microprocessor Address Bus lines A10 and A13-A15 are generated by Microprocessor C2. Bits on lines A13-A15, together with those on AB11-AB12, are the input bits to Address Decoders R1-R2. A10 is exclusive-ORed with BANK SEL by gate B6 to produce the A10 input bit for Random-Access Memory N/P1.

AB0-AB12

Address bits on Buffered Microprocessor Address Bus lines AB0-AB12 are software-generated by Microprocessor C2 and buffered by B1 and C1. These signals are the input bits to Read-Only Memories D1, E/F1, H1, J1, K/L1, and M1; and to Random-Access Memory N/P1.

Address bits AB6-AB8 are the select input signals for Address Decoder P3.

Address bits AB11-AB12 and A13-A15 are the input bits for Address Decoders R1 and R2.

Address bits AB0-AB13 are applied with bits from AVG0-AVG12 to Vector Address Selectors K8, M8, L8, and N8 to produce the data on lines AM0-AM12.

Bits AB0-AB3 are control signals to custom audio chips B3 and C/D3 in the Option Switch Input and Audio Output circuit.

Bits AB0-AB5 are the input signals to latch P2 in the High-Score Table circuit where they are used to produce the A1-A5 address input for EAROM M2.

$\overline{AB13}$

$\overline{AB13}$ is from AB13, inverted by J3, and applied to Vector Address Selector M8. When $\overline{VMEM}$ is low, $\overline{AB13}$ and $\overline{AB12}$ select the specific Vector Memory Read-Only Memory.

AM0-AM13

Address bits on Multiplexed Address Bus lines AM0-AM13 are software-generated by Vector Address Selectors K8, L8, M8, and N8. When $\overline{VMEM}$ is low, the Multiplexed Address Bus is from Buffered Microprocessor Address Bus AB0 through AB12 and $\overline{AB13}$. When $\overline{VMEM}$ is high, AM0-AM12 is from Vector-Generator Address Bus lines AVG0-AVG13.

Signals AM0-AM11 are the input address signals to Vector Read-Only Memories L7, M/N7, N/P7, R7 and to Vector Random-Access Memory K7. In addition, AM11-AM13 are the select input signals for Vector Address Decoder J7. AM0-AM7 are input signals for multiplexers N3 and R3 of the State Machine circuit.

AUD 1-AUD 2

The Audio 1 and Audio 2 signals are game PCB output signals that are generated by custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit. AUD 1 is the inverse of AUD 2. These signals are applied to the Audio/Regulator II PCB and ultimately drive speakers 1 and 2.

AVG0-AVG13

Address bits on Vector-Generator Address Bus lines AVG0-AVG13 are software-generated by Vector Address Controller J9. When $\overline{VMEM}$ is high, these signals are passed through the Vector Address Selectors on lines AM0-AM13 to the Vector Read-Only Memory and the Vector Random-Access Memory.

BANK SEL

The Bank Select signal is developed from data on line DB2. When latch R9 of the Coin Door and Control Panel Output circuit is clocked by $\overline{LATCH}$, R9 latches the data on DB2 to pin 2 of R9, producing the BANK SEL signal. BANK SEL is exclusive-ORed with the address bit A10 by gate B6 to produce input address bit A10 for Random-Access Memory N/P1.

BLANK

Blank is an active high-level signal generated by counter M3 in the Z Intensity and Blanking circuit and ORed with Z BLANK by gate M5 of the R-G-B Output circuit. When high, BLANK turns off transistors Q6, Q8, and Q10, which kills the RED, GREEN, and BLUE output signals to the display.

BLUE

Blue is a game PCB output signal developed from the data on line DVY0. When the data bit on DVY0 is high and latch K10 of the R-G-B Output circuit is clocked by $\overline{STATCLK}$, the data on DVY0 is inverted and latched to pin 11 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q10. Transistor Q10 generates the BLUE signal for the display.

$\overline{BUFFEN}$

Buffer Enable is an active low-level signal developed from $\overline{B\Phi 2}$ by Vector Address Selector K8. $\overline{BUFFEN}$ is the enable input signal for Vector Memory Data Buffer P8. When low, $\overline{BUFFEN}$ allows P8 to pass data.

BΦ2

The active high-level Phase 2 Clock signal is hardware-generated from the internal clock circuitry of Microprocessor C2, buffered by B1, and applied to AND gate K4. Gate K4 ANDs together BΦ2, R/$\overline{WB}$, and 3 MHz to produce $\overline{WRITE}$. BΦ2 is also used as the clock signal for custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit.

$\overline{B\Phi 2}$

The active low-level Phase 2 Clock signal is generated at pin 12 of F3 by inverting BΦ2. $\overline{B\Phi 2}$ is applied to Vector Address Selector K8 to produce $\overline{BUFFEN}$.

$\overline{CENTER}$

Center is an active-low level signal software-generated by gating $\overline{CNTR}$ with $\overline{HALT}$ by Center Flag gate L6. When low, $\overline{CENTER}$ closes switches E10 of the Y-Axis Output circuit and B10 of the X-Axis Output circuit to center the beam on the display.

CNTR

The active high-level Center Flag signal is software-generated by latch E5 of the Center Flag circuit. CNTR is set high when VGCK, $\overline{STROBE3}$, and $\overline{OP2}$ are low. CNTR is applied to gate J5 of the Normalization Flag circuit to develop the clear signal for latch A6. CNTR is ORed with VCTR by GO Flag gate M5 to generate the GO signal.

$\overline{CNTR}$

The active low-level Center Flag signal is software-generated by latch E5 of the Center Flag circuit. When clocked by the 12-MHZ signal, E5 latches $\overline{STOP}$ to pin 9 to produce $\overline{CNTR}$. $\overline{CNTR}$ is gated with $\overline{HALT}$ by Center Flag gate L6 to generate $\overline{CENTER}$.

COIN CNTR-L

Coin Counter Left is a game PCB output signal developed from the data bit on line DB1. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB1 to pin 6 of R9. From here, the signal is current amplified and inverted by Q4 and applied to the game Utility Panel to activate the Left Coin Counter.

COIN CNTR-R

Coin Counter Right is a game PCB output signal developed from the data bit on line DB0. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB0 to pin 5 of R9. From here, the signal is current amplified and inverted by Q3 and applied to the game Utility Panel to activate the Right Coin Counter.

COIN LOCKOUT

Coin Lockout is a game PCB output signal developed from the data on line DB3. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB3 to pin 9 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Right and Left Lockout Coils of the game Coin Door.

D0-D7

Microprocessor Data Bus lines D0-D7 form a bi-directional data bus between the Microprocessor, the Read-Only Memory, and the Option Switch Input circuits.

DB0-DB7

Buffered Microprocessor Data Bus lines DB0-DB7 form a buffered bi-directional data bus between microprocessor data-bus buffer F2 and Vector Memory Data Buffer P8; Coin-Door and Control Panel Input circuit buffers L9, M9, and N9; High-Score Table latches K2 and J2; and High-Score Table buffer H2.

$\overline{DIS\ DAT}$

Disable Data is an active low-level signal generated by test equipment connected to the $\overline{DIS\ DAT}$ test point. $\overline{DIS\ DAT}$ is ANDed with the ROM signal by gate E3 to produce the enable signal for buffer E2 of the Read-Only Memory circuit. When enabled, buffer E2 passes data from the selected Read-Only Memory to the Microprocessor Data Bus.

$\overline{DISRST}$

Display Reset is an active low-level signal software-generated by gate L6 of the Halt Flag circuit. When either $\overline{RESET}$ or $\overline{VGRST}$ is low, $\overline{DISRST}$ is set low. When low, $\overline{DISRST}$ clears State Machine latch P4, DAC Reference and Bipolar Current Sources latch E8, R-G-B Output latch K10, Vector Scaling latch D7, Z Intensity and Blanking latch E6 and counter M3. In addition, $\overline{DISRST}$ presets the HALT signal from latch L5 to the high level.

DVG0-DVG7

Data bits on Vector-Generator Data Bus lines DVG0-DVG7 are software-generated by the selected Vector Read-Only Memory or Vector Random-Access Memory. If Vector Memory Data Buffer P8 is enabled ($\overline{BUFFEN}$ is low) and the R/$\overline{WB}$ line is low, the data on lines DVG0-DVG7 is passed through P8 to the Buffered Microprocessor Data Bus to be read by the microprocessor. Otherwise, the data on DVG0-DVG7 is sent to the Vector Data Shifters and to the Op Code and Intensity Latches.

DVX3-DVX12, $\overline{DVX12}$

Data bits on X-Axis Vector Data lines DVX3-DVX12 and $\overline{DVX12}$ are software-generated by Vector Data Shifters A8, B8, C8, and by latch C6 of the Op Code and Intensity Latches circuit. DVX3-DVX11 and $\overline{DVX12}$ are the input signals to digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit. The data carried on these lines represents the X-axis change from the current location of the display beam. If $\overline{DVX12}$ is low, DAC A/B9 operates only in its lower 512 positions, which means a negative direction of change on the display. If $\overline{DVX12}$ is high, DAC A/B9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVX11 and DVX12 are exclusive-ORed by gate B6 of the Normalization Flag circuit.

DVY0-DVY12, $\overline{DVY12}$

Data bits on Y-Axis Vector Data lines DVY0-DVY12 and $\overline{DVY12}$ are software-generated by Vector Data Shifters F8, H8, J8, and by latch D6 of the Op Code and Intensity Latches circuit. DVY3-DVY11 and $\overline{DVY12}$ are the input signals for digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit. The data carried on these lines represents the Y-axis change from the current location of the display beam. If $\overline{DVY12}$ is low, DAC F9 operates only in its lower 512 positions, which means a negative direction of change on the display. If $\overline{DVY12}$ is high, DAC F9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVY0-DVY7 are applied to latch E8 in the DAC Reference and Bipolar Current Sources circuit. These signals, together with VCTR and $\overline{VCTR}$, set the X REF and Y REF voltage levels (via DAC D9).

Lines DVY0-DVY2 carry data representing the eight different color signals for latch K10 of the R-G-B Output circuit.

Lines DVY4-DVY7 carry data representing the Z-intensity signals for latch E6 of the Z Intensity and Blanking circuit.

Data on DVY8-DVY10 are applied to latch D7 of the Vector Scaling circuit. The data carried on these lines represents the number (in binary) that the Vector Scaling circuit uses to divide into the vector drawing time. The vector drawing time n is divided by 2 , where n equals the number represented on DVY8-DVY10.

In addition, DVY11 and DVY12 are exclusive-ORed by gate B6 of the Normalization Flag circuit.

$\overline{EAROMCON}$

The Electrically-Alterable ROM Control signal is an active low-level signal software-generated by Address Decoder P3 at address 8900. $\overline{EAROMCON}$ is the clock signal for latch K2 in the High-Score Table circuit. $\overline{EAROMCON}$ allows K2 to pass data bits on lines DB0-DB3 to the control lines of EAROM M2.

$\overline{EAROMRD}$

The Electrically-Alterable ROM Read Enable is an active low-level signal software-generated by Address Decoder R2 at address 7000. $\overline{EAROMRD}$ is the read-enable signal for buffer H2 of the High-Score Table circuit. $\overline{EAROMRD}$ allows the eight data bits from EAROM M2 to be passed through buffer H2 to the microprocessor data bus.

$\overline{EAROMWR}$

The Electrically-Alterable ROM Write Enable is an active low-level signal software-generated by Address Decoder P3 at address 8940. $\overline{EAROMWR}$ is the clock signal for latches J2 and P2 in the High-Score Table circuit. $\overline{EAROMWR}$ allows address bits on lines AB0-AB5 and data bits on lines DB0-DB7 to pass to the address and data input pins of EAROM M2.

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Description of Gravitar PCB Signal Names (continued)

ENORM

The active low-level Normalization Flag is software-generated by gate K4 of the Normalization Flag circuit. If OP0 is high, SA is high, and the output from gate J5 is high, ENORM is set low when STROBE0 goes high. ENORM is applied through gate E7 to the S1 input pins of Vector Data Shifters A8, B8, C8, F8, H8, and J8. ENORM multiples the rate of change of the X and Y vector data in the Vector Data Shifters (via shift left operations) at the same 2^n factor specified by data on lines DVY8-DVY10. The n number is incremented at a 12-MHz rate until either DVX11 or DVY11 changes state, which then sets ENORM to the high level.

GO

The Go flag is an active high-level signal software-generated by gate M5 of the Go Flag circuit when either VCTR or CNTR are high. GO is gated with HALT* by gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM N4.

GO is also used as the enable signal for Vector Timer R6. When GO is high, the Vector Timer starts its count. The Vector Timer counts to 256 if OP1 is high and OP1 is low. If OP1 is low and OP1 is high, the Vector Timer counts to 16K.

GREEN

Green is a game PCB output signal developed from the data on line DVY1 in the R-G-B Output circuit. When DVY1 is high and latch K10 is clocked by STATCLK, the data bit on DVY1 is inverted and latched to pin 6 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q8. Transistor Q8 generates the GREEN signal for the display.

HALT

The active high-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. HALT is applied through buffer M9 of the Coin Door and Control Panel Input circuit (when SINP1 is low) to permit Microprocessor C2 to read the status of HALT on line DB6. In addition, HALT is applied to latch P4 of the State Machine circuit to develop HALT*.

HALT*

The active high-level Delayed Halt Flag is software-generated by latch P4 of the State Machine circuit. HALT* is generated when the HALT signal has been delayed by one pulse of inverted VGCK (1.5 MHz), which in turn has been delayed by one pulse of 12 MHz. HALT* is ORed with GO by gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM N4.

HALT

The active low-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. HALT is the clear signal for Vector Flag latch E5 and Center Flag latch E5. In addition, HALT is ORed with CNTR by gate L6 of the Center Flag circuit to produce CENTER.

INTACK

Interrupt Acknowledge is an active low-level signal software-generated from Address Decoder P3 at address 88C0. This signal is an acknowledgment from Microprocessor C2 that an interrupt request has been received. INTACK resets counter J4.

INVERT X

Invert X is an active high-level signal developed from the data bit on line DB6. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB6 to pin 12 of R9. When high, INVERT X closes switch B10 through inverter K9 in the X-Axis Output circuit. This inverts the X-axis vector instruction to the display.

INVERT Y

Invert Y is an active high-level signal developed from the data bit on line DB7. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches DB7 to pin 15 of R9. When high, INVERT Y closes switch E10 through inverter K9 in the Y-Axis Output circuit. This inverts the Y-axis vector instruction to the display.

IO

The Input/Output signal is an active low-level signal software-generated by Address Decoder R2 during addresses 8000 through 8FFF. IO is gated with R/WB by gate J6 to produce the direction signal for bi-directional data buffer N9 of the Coin Door and Control Panel Input circuit. IO determines the direction of data flow through buffer N9.

I/OS

I/OS is an active high-level signal software-generated from Address Decoder R2 during addresses 6000 through 6FFF. The I/OS signal is ORed with the ROM signal by gate R4 to enable bi-directional data bus buffer F2 to pass data. When I/OS is high, data buffer F2 is turned off, which allows custom audio chips B3 and C/D3 to pass data to the data bus.

I/O0

I/O0 is an active low-level signal software-generated by Address Decoder R2 at address 6800. I/O0 is the chip-select enable for custom audio chip C/D3 in the Option Switch Input and Audio Output circuit.

I/O1

I/O1 is an active low-level signal software-generated by Address Decoder R2 at address 6000. I/O1 is the chip-select enable for custom audio chip B3 in the Option Switch Input and Audio Output circuit.

LATCH

Latch is an active low-level signal generated by Address Decoder P3 at address 8800. LATCH is the clock signal for latch R9 in the Coin Door and Control Panel Output circuit. When low, LATCH allows the data bits on lines DB0-DB7 to pass through R9.

LATCH0

Latch 0 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH0 is applied through inverter F7 to the S0 input pins of shift registers F8 and J8 in the Vector Data Shifters circuit. LATCH0 causes the data bits on lines DVG0-DVG7 to be latched by F8 and J8 to lines DVY0-DVY7 when F8 and J8 are clocked by the 12-MHz clock signal.

LATCH1

Latch 1 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH1 is applied through inverter F7 to the S0 input pin of shift register H8 in the Vector Data Shifters circuit. LATCH1 causes the data bits on lines DVG0-DVG3 to be latched by H8 to lines DVY8-DVY10 when H8 is clocked by the 12-MHz clock signal.

LATCH1 is also the clear signal for Vector Data Shifters A8, B8, C8, F8, J8, and for Op Code and Intensity Latch C6.

In addition, LATCH1 is the clock signal for Op Code and Intensity Latch D6. When LATCH1 goes low, the data bits on lines DVG4-DVG7 are latched by D6 to lines OP0-OP2, OP0-OP2, DVY12, and DVY12.

LATCH2

Latch 2 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH2 is applied through inverter F7 to the S0 input pins of shift registers A8 and C8 in the Vector Data Shifters circuit. LATCH2 causes the data bits on lines DVG0-DVG7 to be latched by A8 and C8 to lines DVX3-DVX7 when A8 is clocked by the 12-MHz clock signal.

LATCH3

Latch 3 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH3 is applied through inverter F7 to the S0 input pin of shift register B8 in the Vector Data Shifters circuit. LATCH3 causes the data bits on lines DVG0-DVG3 to be latched by B8 to lines DVX8-DVX11 when B8 is clocked by the 12-MHz clock signal.

LATCH3 is also the clock signal for Op Code and Intensity Latch C6. When LATCH3 goes low, the data bits on lines DVG4-DVG7 are latched by C6 to lines Z0-Z2, Z1-Z2, DVX12, and DVX12.

NORM

The active high-level Normalization Flag is software-generated by latch A6 in the Normalization Flag circuit. If OP0 is high, NORM is set high when STROBE0 goes high. NORM is gated with SCALE by gate K5 in the Vector Timer circuit to produce the load-enable signal for Vector Timers M6, N6, P6, and R6. If the Vector Timers are enabled, NORM initiates the divide-by-2^n operation of the vector drawing time. (The n factor is specified by the data on lines DVY8-DVY10 to Vector Scaling latch D7.)

OPTION 0-OPTION 2

The Option 0, Option 1, and Option 2 signals are hardware-generated by DIP switch P10. They are applied to switch input buffer L9 of the Coin Door and Control Panel Input circuit. When L9 is enabled by SINP2, OPTION 0-OPTION 2 are passed to Buffered Microprocessor Data Bus lines DB5-DB7.

OP0

The Op Code 0 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG5 is high, OP0 is set high when D6 is clocked by LATCH1. OP0 is multiplexed with AM4 by N3 in the State Machine circuit to produce the A4 input address bit for State Machine ROM N4.

If OP0 is high, HALT from Halt Flag latch L5 is set high when L5 is clocked by STROBE3.

If OP0, OP2, STROBE3, and VGCK are all low, VCTR from Vector Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

OP0

The Complementary Op Code 0 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP0. If OP0 is low, NORM from Normalization Flag latch A6 is set high when STROBE0 clocks A6. OP0 is also the OP0 and OPX input signal for Vector Address Controller J9.

OP1

The Op Code 1 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG6 is high, OP1 is set high when D6 is clocked by LATCH1. OP1 is multiplexed with AM5 by N3 in the State Machine circuit to produce the A5 input address bit for State Machine ROM N4. In addition, OP1 is the OP1 signal for Vector Address Controller J9.

In the Vector Timer circuit, OP1 is gated by K5 and E3 to enable a 1 to be loaded into the D input pin of Vector Timer P6 (if NORM or SCALE is low).

OP1

The Complementary Op Code 1 signal is sofware-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP1. OP1 is the clear signal for Vector Timers N6 and M6. When OP1 goes low, the count from N6 and M6 is stopped, causing a lowered count from the Vector Timer circuit. This low count is used to draw short vectors on the display. OP1 is also gated with the outputs of the Vector Timers by gates L3 and H3 to set STOP to the low level.

OP2

The Op Code 2 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG7 is high, OP2 is set high when D6 is clocked by LATCH1. OP2 is multiplexed with AM6 by N3 in the State Machine circuit to produce the A6 input address bit for State Machine ROM N4.

If OP2, OP0, STROBE3, and VGCK are all low, VCTR from Vector Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

When STROBE1 goes low, if OP2 is low, it is applied through gates B7 and F3 of the Vector Scaling circuit as the load signal for counter C7. This allows the data latched from DVY8-DVY10 by D7 to be loaded into counter C7. When STROBE1 goes high, counter C7 counts down until it reaches the minimum count. At the same time, the Vector Timer circuit does a divide-by-2 (shift right) operation for each count of C7. (This is caused by SCALE being at the high state.) When C7 reaches its minimum count, it sets pin 12 high, dropping SCALE to the low state.

If OP2 and DVY12 are low, SCALELD from gate J6 is set low when STROBE2 goes low. This allows Vector Scaling latch D7 to latch the new data on DVY8-DVY10.

If OP2 and DVY12 are low, STATCLK from J6 is set low when STROBE2 goes low. This allows latch E6 of the Z Intensity and Blanking circuit to latch the data on DVY4-DVY7.

OP2

The Complementary Op Code 2 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP2. If OP2, STROBE3, and VGCK are low, CNTR from Center Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal. OP2 is also ORed with SA by gate R4 to produce the OP2 input for Vector Address Controller J9.

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Description of Gravitar PCB Signal Names (continued)

PLAYER 1 LED

The Player 1 LED On signal is developed from the data bit on line DB4. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on line DB4 to pin 19 of R9. This signal is applied through R103 to light the Player 1 LED on the game Control Panel.

PLAYER 2 LED

The Player 2 LED On signal is developed from the data bit on line DB5. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB5 to pin 16 of R9. This signal is applied through R102 to light the Player 2 LED on the game Control Panel.

POR

The active high-level Power-On Reset signal is hardware-generated at pin 4 of F7 in the Power-On Reset circuit. POR is the clock signal that starts the count of E4 of the Clock circuit.

$\overline{\text{POR}}$

The active low-level Power-On Reset signal is hardware-generated at pin 6 of inverter F7 in the Power-On Reset circuit. $\overline{\text{POR}}$ is generated when the voltage at pin 3 of R8 is less than about 7 volts or when the RESET test point is shorted to ground. $\overline{\text{POR}}$ is developed into the $\overline{\text{RESET}}$ signal to protect Microprocessor C2.

$\overline{\text{RAM}}$

The Random-Access Memory Enable is an active low-level signal software-generated by Address Decoder R2 during addresses 0000 through 07FF. $\overline{\text{RAM}}$ is the chip-enable signal for Random-Access Memory N/P1. When low, $\overline{\text{RAM}}$ allows data to be read from or written to N/P1, depending upon the state of $\overline{\text{WRITE}}$.

RED

Red is a game PCB output signal developed from the data on line DVY2 in the R-G-B Output circuit. When DVY2 is high and latch K10 is clocked by $\overline{\text{STATCLK}}$, the data bit on DVY2 is inverted and latched to pin 3 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q6. Transistor Q6 generates the RED signal for the display.

$\overline{\text{RESET}}$

Reset is an active low-level signal generated at pin 6 of K3 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets $\overline{\text{RESET}}$ to an active low level either when the RESET test point is shorted to ground or during the time that the power-supply voltages are reaching their stabilized, regulated levels. This ensures that the Microprocessor Address Bus is stabilized before the microprocessor begins operation.

The Watchdog circuit sets $\overline{\text{RESET}}$ to an active low level if the microprocessor fails to output address 0D00 before Watchdog counter H4 has reached its maximum count.

$\overline{\text{RESET}}$ is also the clear signal for latch R9 in the Coin Door and Control Panel Output circuit.

In addition, RESET is gated with $\overline{\text{VGRST}}$ by gate L6 in the Halt Flag circuit to produce $\overline{\text{DISRST}}$.

ROM

The Read-Only Memory Enable is an active high-level signal software-generated from Address Decoder R1 during addresses 9000 through 9FFF. ROM is ORed with $\overline{\text{I/OS}}$ by gate R4 to enable bi-directional data bus buffer F2 to pass data.

In addition, ROM is ANDed with $\overline{\text{DIS DAT}}$ to enable data buffer E2.

$\overline{\text{ROM0}}$

Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Address Decoder R1 at addresses 9000-9FFF. $\overline{\text{ROM0}}$ is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM0}}$ allows ROM D1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM1}}$

Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Address Decoder R1 at addresses A000-AFFF. $\overline{\text{ROM1}}$ is the chip-select signal for ROM E/F1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM1}}$ allows ROM E/F1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM2}}$

Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Address Decoder R1 at addresses B000-BFFF. $\overline{\text{ROM2}}$ is the chip-select signal for ROM H1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM2}}$ allows ROM H1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM3}}$

Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Address Decoder R1 at addresses C000-CFFF. $\overline{\text{ROM3}}$ is the chip-select signal for ROM J1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM3}}$ allows ROM J1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM4}}$

Read-Only Memory Chip Select 4 is an active low-level signal software-generated by Address Decoder R1 at addresses D000-DFFF. $\overline{\text{ROM4}}$ is the chip-select signal for ROM K/L1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM4}}$ allows ROM K/L1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM5}}$

Read-Only Memory Chip Select 5 is an active low-level signal software-generated by Address Decoder R1 at addresses E000-EFFF. $\overline{\text{ROM5}}$ is the chip-select signal for ROM M1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM5}}$ allows ROM M1 to be addressed and to pass data to buffer E2.

R/$\overline{\text{WB}}$

The Buffered Read/Write Enable is generated by Microprocessor C2, buffered by B1, and applied as the read/write enable signal for custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit. In the high state, R/$\overline{\text{WB}}$ is the read enable for the custom audio chips; in the low state, it is the write enable for these chips.

$\overline{\text{R}}$/WB

The Buffered Read/Write Eanble is generated at pin 2 of F3 in the Microprocessor circuit by inverting R/$\overline{\text{WB}}$. $\overline{\text{R}}$/WB is ANDed with BΦ2 and 3 MHz by gate K4 to produce $\overline{\text{WRITE}}$. $\overline{\text{R}}$/WB is the direction signal for Vector Memory Data Buffer P8 and determines the direction of data flow through P8. In the high state, $\overline{\text{R}}$/WB allows data to pass through P8 from the data bus to the vector generator data bus; in the low state, it allows data to pass in the reverse direction.

SA

The active high-level Signature Analysis Flag signal is hardware-generated at pin 12 of inverter J3 when test point $\overline{\text{SA}}$ at pin 13 is grounded. SA is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

$\overline{\text{SA}}$

The active low-level Signature Analysis Flag is hardware-generated when test point $\overline{\text{SA}}$ at pin 13 of J3 is grounded. $\overline{\text{SA}}$ is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

SACLK

Signature Analysis Clock is a test point at pin 8 of gate B7 in the State Machine Clock Logic circuit. SACLK is used to apply the clock signal from the Signature Analyzer or ATARI CAT Box for the reading of game PCB signatures.

SAEN

Signature Analysis Enable is a test point at pin 8 of gate M5 in the Vector Address Selector circuit. SAEN is generated by gating $\overline{\text{VRAM}}$ with the data bit on line AM10 by gates J3 and M5. SAEN is used to enable a Signature Analyzer or the ATARI CAT Box for the reading of game PCB signatures.

SCALE

Scale is an active high-level signal generated by gate B7 of the Vector Scaling circuit. When OP2 is high and counter C7 is counting down, SCALE is set high. SCALE is ORed with NORM by gate K5 of the Vector Timer circuit to produce the load signal for Vector Timers M6, N6, P6, and R6. When SCALE is high, the Vector Timers perform a load operation for each count of C7 (at a 12-NHz rate). This results in a vector drawing time divided by a factor of 2^n, where n equals the total counts of C7. When C7 reaches its minimum count, SCALE is set low.

SCALE is gated with VCTR, CNTR, DVY11-DVY12, and DVX11-DVX12 of the Normalization Flag circuit to produce the clear signal for latch A6.

$\overline{\text{SCALELD}}$

Scale Load is an active low-level signal software-generated by gates N5, L3, and L6 of the Vector Generator circuit. When $\overline{\text{STROBE2}}$, OP2, and $\overline{\text{DVY12}}$ are all low, $\overline{\text{SCALELD}}$ is set low. $\overline{\text{SCALELD}}$ is the clock signal for Vector Scaling latch D7. When $\overline{\text{SCALELD}}$ goes high, the data on lines DVY8-DVY10 are latched to the output pins of D7.

$\overline{\text{SINP1}}$

Switch Input 1 is an active low-level signal software-generated by Address Decoder R2 at address 7800. $\overline{\text{SINP1}}$ is the direction signal for bi-directional data buffer M9 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer M9.

$\overline{\text{SINP2}}$

Switch Input 2 is an active low-level signal software-generated by Address Decoder R2 at address 8000. $\overline{\text{SINP2}}$ is the direction signal for bi-directional data buffer L9 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer L9.

$\overline{\text{STATCLK}}$

State Clock is an active low-level signal software-generated by gates N5, L3, and J6 of the Vector Generator circuit. When $\overline{\text{STROBE2}}$, OP2, and DVY12 are all low, $\overline{\text{STATCLK}}$ is set low. $\overline{\text{STATCLK}}$ is the clock for latch K10 in the R-G-B Output circuit and latch E6 in the Z Intensity and Blanking circuit. When $\overline{\text{STATCLK}}$ goes high, the data bits on DVY0-DVY2 are latched by K10, and those on DVY4-DVY7 are latched by E6.

$\overline{\text{STOP}}$

Stop is an active low-level signal generated by gate H3 of the Vector Timer circuit. $\overline{\text{STOP}}$ is set low when Vector Timers N6, M6, P6, and R6 have reached their maximum count. If $\overline{\text{STOP}}$ is low, VCTR from Vector Flag latch E5 and CNTR from Center Flag latch E5 are both set low when E5 is clocked by the 12-MHz clock signal.

$\overline{\text{STROBE0}}$

Strobe 0 is an active low-level signal software-generated by State Machine decoder H7. $\overline{\text{STROBE0}}$ is the clock signal for Normalization Flag latch A6. It is also the $\overline{\text{STROBE0}}$ input for Vector Address Controller J9.

$\overline{\text{STROBE1}}$

Strobe 1 is an active low-level signal software-generated by State Machine decoder H7. If OP2 is low, when $\overline{\text{STROBE1}}$ goes low, the data latched at the outputs of D7 in the Vector Scaling circuit are loaded into counter C7. When $\overline{\text{STROBE1}}$ goes high, C7 begins counting down.

$\overline{\text{STROBE1}}$ is the $\overline{\text{STROBE1}}$ input for Vector Address Controller J9.

$\overline{\text{STROBE2}}$

Strobe 2 is an active low-level signal software-generated by State Machine decoder H7. If OP2 and $\overline{\text{DVY12}}$ are both low, $\overline{\text{SCALELD}}$ from gate J6 is set low when $\overline{\text{STROBE2}}$ goes low. If OP2 and DVY12 are both low, $\overline{\text{STATCLK}}$ is set low when $\overline{\text{STROBE2}}$ goes low.

$\overline{\text{STROBE2}}$ is the $\overline{\text{STROBE2}}$ input for Vector Address Controller J9.

$\overline{\text{STROBE3}}$

Strobe 3 is an active low-level signal software-generated by State Machine decoder H7. $\overline{\text{STROBE3}}$ is the clock signal for Halt Flag latch L5 and is the $\overline{\text{STROBE3}}$ input for Vector Address Controller J9.

If OP0, OP2, $\overline{\text{OP2}}$, and VGCK are all low, VCTR from Vector Flag latch E5 and CNTR from Center Flag latch E5 are both set high when $\overline{\text{STROBE3}}$ goes low.

ST0-ST2

State signals ST0-ST2 are active high-level signals that are software-generated by State Machine ROM N4. These signals, together with ST3, are decoded by H7 of the State Machine circuit to produce $\overline{\text{LATCH0}}$-$\overline{\text{LATCH3}}$ and $\overline{\text{STROBE0}}$-$\overline{\text{STROBE3}}$. ST2 is used to develop ST3 and is also the ST2 input for Vector Address Controller J9.

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Description of Gravitar PCB Signal Names (continued)

ST3

State signal ST3 is an active high-level signal hardware-generated by Decoder Disable latch A7. ST3 is opposite in state to VGCK, and is delayed by one pulse of the 12-MHz clock signal if the Q4 output from State Machine ROM N4 is low and $\overline{VMEM}$ is high. If the Q4 output from N4 is high, ST3 is high. When ST3 is high, State Machine decoder H7 is disabled. When ST3 is low, H7 decodes the data on lines ST0-ST2 to produce $\overline{LATCH0}$-$\overline{LATCH3}$ and $\overline{STROBE0}$-$\overline{STROBE3}$.

VCTR, $\overline{VCTR}$

The Vector Flag signals are software-generated by Vector Flag latch E5. If OP0, OP2, $\overline{STROBE3}$, and VGCK are low and $\overline{HALT}$ is high, VCTR is set high and $\overline{VCTR}$ is set low when E5 is clocked by the 12-MHz clock signal. VCTR is ORed with CNTR by gate M5 to set GO high.

SCALE, CNTR, DVY11-DVY12, and DVX11-DVX12 are gated with VCTR to produce the clear signal for Nomalization Flag latch A6.

In the Z Intensity and Blanking circuit, VCTR is the clock signal for latch H6 and the serial input signal for shift register M3.

VCTR and $\overline{VCTR}$ are used by the DAC Reference and Bipolar Current Sources circuit to set the X BIP, Y BIP, X REF, and Y REF levels.

VGCK

The Vector Generator clock signal is generated at pin 18 of buffer B1 in the Microprocessor circuit. VGCK is derived from the 1.5 MHz clock signal and is applied to AND gate J5 of the State Machine Clock Logic circuit. VGCK is the basic timing signal of the State Machine circuit.

$\overline{VGGO}$

The Vector Generator Go signal is an active low-level signal software-generated by Address Decoder P3 at address 8840. $\overline{VGGO}$ is the clear signal for latch L5 of the Halt Flag circuit. When low, $\overline{VGGO}$ sets HALT to the inactive low level.

$\overline{VGRST}$

Vector Generator Reset is an active low-level signal software-generated by Address Decoder P3 at address 8880. $\overline{VGRST}$ is ORed with $\overline{RESET}$ by gate L6 of the Halt Flag circuit to produce $\overline{DISRST}$.

$\overline{VMEM}$

The Vector Memory Select Enable is an active low-level signal software-generated by Address Decoder R1 during addresses 2000 through 5FFF. $\overline{VMEM}$ is the select-enable signal for Vector Address Selectors K8, L8, M8, and N8. When low, $\overline{VMEM}$ allows the Vector Address Selectors to produce $\overline{VW}$, $\overline{BUFFEN}$, and the AM0-AM12 multiplexed address bits. $\overline{VMEM}$ is also applied to gate K5 of the State Machine Clock Logic circuit where it is used to generate ST3.

$\overline{VRAM}$

The Vector Random-Access Memory Chip Enable is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2000-27FF. When low, $\overline{VRAM}$ enables Vector Random-Access Memory K7 to be addressed to either receive or transmit data, depending upon the state of $\overline{VW}$. $\overline{VRAM}$ is also used to produce the SAEN signal from M5 of the Vector Address Selector circuit.

$\overline{VROM0}$

Vector Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2800-2FFF. $\overline{VROM0}$ is the chip-select signal for ROM L7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM0}$ allows ROM L7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VROM1}$

Vector Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 3000-3FFF. $\overline{VROM1}$ is the chip-select signal for ROM M/N7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM1}$ allows ROM M/N7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VROM2}$

Vector Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 4000-4FFF. $\overline{VROM2}$ is the chip-select signal for ROM N/P7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM2}$ allows ROM N/P7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VROM3}$

Vector Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 5000-5FFF. $\overline{VROM3}$ is the chip-select signal for ROM R7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM3}$ allows ROM R7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VW}$

The Vector Write Enable is an active low-level signal software-generated from Vector Address Selector K8, ANDed with $\overline{B\Phi 2}$ by gate J6, and applied as the write-enable signal for Vector Random-Access Memory K7. When low, $\overline{VW}$ allows data to be written to K7; when high, $\overline{VW}$ permits data to be read from K7.

$\overline{WDCLR}$

Watchdog Clear is an active low-level signal software-generated by Address Decoder P3 at address 8980. $\overline{WDCLR}$ is ORed with $\overline{POR}$ by gate E3 to clear the count of Watchdog counter H4.

$\overline{WDDIS}$

Watchdog Disable is a test point at pin 9 of AND gate L4 in the Watchdog circuit. When $\overline{WDDIS}$ is grounded, $\overline{RESET}$ is prevented from going to an active low level (except when the RESET test point is grounded).

$\overline{WRITE}$

Write Enable is an active low-level signal generated by gate K4 of the Microprocessor circuit. $\overline{WRITE}$ is used to enable Address Decoder P3 and Random-Access Memory N/P1. $\overline{WRITE}$ is also applied to pin 11 of K8 in the Vector Address Selector circuit to develop $\overline{VW}$.

X BIP

The X-Axis Bipolar Current is set by R99 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

X OUT

X Output is a game PCB output signal generated by the X-Axis Output circuit. X OUT carries the horizontal beam deflection signal for the drawing of vectors on the display.

X REF

The X-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

Y BIP

The Y-Axis Bipolar Current is set by R98 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Y OUT

Y Output is a game PCB output signal generated by the Y-Axis Output circuit. Y OUT carries the vertical beam deflection signal for the drawing of vectors on the display.

Y REF

The Y-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Z0-Z2, $\overline{Z1}$-$\overline{Z2}$

Z Intensity signals Z0-Z2 and $\overline{Z1}$-$\overline{Z2}$ are software-generated by latch C6 in the Op Code and Intensity Latches circuit. These signals are derived from the data on lines DVG51-DVG7 when C6 is clocked by $\overline{LATCH3}$. If the binary count carried by Z0-Z2 is not equal to 1, these signals are the input signals for latch F6 in the Z Intensity and Blanking circuit. If the binary count carried by Z0-Z2 is 1, Z Intensity signals Z0, $\overline{Z1}$, and $\overline{Z2}$ are ANDed by gate F5 of the Z Intensity and Blanking circuit to produce the select signal for latch F6. This select signal causes the latched data from E6 to be applied as the input signals for latch F6.

Z OUT

Z Intensity Output is a game PCB output signal generated by the Z Intensity and Blanking circuit from either DVY4-DVY7 or Z0-Z2. The Q output signals from latch H6 are summed at the base of Q7. Transistors Q7 and Q9 buffer Z OUT before it is sent to the game display circuitry to control the display intensity.

3 KHZ

The 3 kHz clock signal is generated at pin 6 of Clock counter F4 and is applied through switch input buffer M9 of the Coin Door and Control Panel Input circuit (when $\overline{SINP1}$ is low). The 3 kHz clock is read by the microprocessor on data line DB7. This frequency is the time reference for the Microprocessor C2.

12 KHZ

The 12 kHz clock signal is generated at pin 4 of Clock counter F4 and is applied to reset A4 of the High-Score Table.

3 MHZ

The 3 MHz clock signal is generated at pin 2 of Clock counter F4. The 3 MHz signal is ANDed with R/$\overline{WB}$ and BΦ2 by gate K4 to produce $\overline{WRITE}$. It is also applied to AND gate J5 of the State Machine Clock Logic and to shift register M3 of the Z Intensity and Blanking circuit.

6 MHZ

The 6 MHz clock signal is generated at pin 3 of Clock counter F4 and is applied to gate J5 of the State Machine Clock Logic circuit.

12 MHZ

The 12 MHz clock signal is generated at pin 10 of inverter F3 in the Clock circuit. This signal clocks the Vector Timer Shifters, the Vector Flag latch, and the Center Flag latch.

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Gravitar™ PCB Signal Name Descriptions

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Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the game PCB. (Use extender cables, if available.)
6. Connect together the Φ0 and Φ2 test points on the game PCB with the shortest possible jumper.
7. Connect the $\overline{\text{WDDIS}}$ test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST: OFF
    b. TESTER MODE: R/$\overline{\text{W}}$
11. Press TESTER RESET.

B. Address Lines

1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box.
3. Connect the DATA PROBE ground clip to a game PCB ground test point.
4. Set CAT Box switches as indicated:
    a. BYTES: 1
    b. PULSE MODE: UNLATCHED
    c. R/$\overline{\text{W}}$ MODE: (OFF)
    d. R/$\overline{\text{W}}$: WRITE
5. Key in the address pattern given in Table 1 *(use AAAA to start)* with the CAT Box keyboard.
6. Press DATA SET.
7. Key in the data pattern given in Table 1 *(use AA to start)* with the keyboard.
8. Set R/$\overline{\text{W}}$ MODE: STATIC
9. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 1 lights up. Repeat this step for each address line listed in Table 1.
10. Repeat parts 4-c through 9 using address *5555* in part 5 and data *55* in part 7.

C. Data Lines

1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box.

Table 1 Address Lines

When writing *AAAA* pattern	Address lines	When writing *5555* pattern
LOGIC STATE	**IC-PIN**	**LOGIC STATE**
1	R2-12	0
0	R2-13	1
1	R2-14	0
0	B1-5	1
1	B1-7	0
0	B1-12	1
1	B1-14	0
0	B1-16	1
1	C1-9	0
0	C1-7	1
1	C1-5	0
0	C1-3	1
1	C1-12	0
0	C1-14	1
1	C1-16	0
0	C1-18	1

3. Connect the DATA PROBE ground clip to the game PCB ground test point.
4. Set CAT Box switches as indicated:
    a. BYTES:1
    b. R/$\overline{\text{W}}$ MODE: (OFF)
    c. R/$\overline{\text{W}}$: WRITE
5. Key in address *0000* with the keyboard.
6. Press DATA SET.
7. Key in data *AA* with the keyboard.
8. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
9. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this check for each IC-pin in Table 2.
10. Repeat parts 6 through 9 using data *55* in part 7.

D. RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. DBUS SOURCE: ADDR
    b. BYTES:1024
    c. R/$\overline{\text{W}}$ MODE: (OFF)
    d. R/$\overline{\text{W}}$: WRITE
3. Enter address *0000* with the keyboard.
4. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
5. Set R/$\overline{\text{W}}$: READ.
6. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
7. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabl-

MEMORY MAP

HEXA-DECIMAL ADDRESS	ADDRESS BUS A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
E000-EFFF	1	1	1		A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 5}}$
D000-DFFF	1	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 4}}$
C000-CFFF	1	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 3}}$
B000-BFFF	1	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 2}}$
A000-AFFF	1	0	1	0	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 1}}$
9000-9FFF	1	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 0}}$
8800	1	0	0	0	1												R	D								CABINET 1
																			D							$\overline{\text{START 2}}$
																				D						$\overline{\text{START 1}}$
																					D					$\overline{\text{THRUST 2}}$
																						D				$\overline{\text{ROT LEFT 2}}$
																							D			$\overline{\text{ROT RIGHT 2}}$
																								D		$\overline{\text{FIRE 2}}$
																									D	SHIELDS 2
89C0	1	0	0	0	1	0	0	1	1	1							W									$\overline{\text{SPARE WT}}$
8980	1	0	0	0	1	0	0	1	1	0							W									$\overline{\text{WDCLR}}$
8940	1	0	0	0	1	0	0	1	0	1	D	D	D	D	D	D	W	D	D	D	D	D	D	D	D	$\overline{\text{EAROMWR}}$
8900	1	0	0	0	1	0	0	1	0	0							W					D	D	D	D	$\overline{\text{EAROMCON}}$
88C0	1	0	0	0	1	0	0	0	1	1							W									$\overline{\text{INTACK}}$
8880	1	0	0	0	1	0	0	0	1	0							W									$\overline{\text{VGRST}}$
8840	1	0	0	0	1	0	0	0	0	1							W									$\overline{\text{VGGO}}$
8800	1	0	0	0	1	0	0	0	0	0							W	D								INVERT Y
																			D							INVERT X
																				D						$\overline{\text{PLAYER 2 LED}}$
																					D					PLAYER 1 LED
																						D				COIN LOCKOUT
																							D			BANK SEL
																								D		COIN CNTR-L
																									D	COIN CNTR-R
8000	1	0	0	0	0												R	D								OPTION 2
																			D							OPTION 1
																				D						OPTION 0
																					D					$\overline{\text{THRUST 1}}$
																						D				$\overline{\text{ROT LEFT 1}}$
																							D			$\overline{\text{ROT RIGHT 1}}$
																								D		$\overline{\text{FIRE 1}}$
																									D	SHIELDS 1
7800	0	1	1	1	1												R	D								3 KHZ
																			D							HALT
																				D						$\overline{\text{SA}}$
																					D					SELF-TEST
																						D				$\overline{\text{COIN-AUX}}$
																							D			$\overline{\text{COIN L}}$
																								D		$\overline{\text{COIN R}}$
7000	0	1	1	1	0												R	D	D	D	D	D	D	D	D	$\overline{\text{EAROMRD}}$
6800	0	1	1	0	1												R/$\overline{\text{W}}$	D	D	D	D	D	D	D	D	$\overline{\text{I/O0}}$
6000	0	1	1	0	0												R/$\overline{\text{W}}$	D	D	D	D	D	D	D	D	$\overline{\text{I/O1}}$
5000-5FFF	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 3}}$
4000-4FFF	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 2}}$
3000-3FFF	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 1}}$
2800-2FFF	0	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 0}}$
2000-27FF	0	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	R/$\overline{\text{W}}$	D	D	D	D	D	D	D	D	$\overline{\text{VRAM}}$
0000-07FF	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	R/$\overline{\text{W}}$	D	D	D	D	D	D	D	D	$\overline{\text{RAM}}$

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ed. Using this switch, determine if the error is in the high-order or low-order RAM.

8. Repeat parts 2-d through 7 using addresses *0400, 2000,* and *2400* .
9. Repeat this test with DBUS SOURCE set to $\overline{\text{ADDR}}$.

E. Custom Audio I/O Chips

NOTE

Gravitar has two custom audio I/O chips. Each must be tested separately. There are several ways to test these chips:

- Perform the self-test.
- Substitute a known good part for a suspected defective part.
- Use the following procedure.

1. Perform the CAT Box preliminary set-up.

Table 2 Data Lines

When writing *AA* pattern	Data lines	When writing *55* pattern
LOGIC STATE	IC-PIN	LOGIC STATE
1	F2-11	0
0	F2-12	1
1	F2-13	0
0	F2-14	1
1	F2-15	0
0	F2-16	1
1	F2-17	0
0	F2-18	1
1	F2-9	0
0	F2-8	1
1	F2-7	0
0	F2-6	1
1	F2-5	0
0	F2-4	1
1	F2-3	0
0	F2-2	1

2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{\text{W}}$: WRITE
   c. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 3 with the keyboard.
6. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
7. Repeat parts 3 through 6 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

ADDRESS	DATA	TEST RESULTS
680F	*00*	
680F	*03*	
6800	*55*	
6801	*AF*	Custom Audio I/O Chip B3 channel 1 produces pure tone.
6801	*00*	Custom Audio I/O Chip B3 channel 1 off.
6802	*55*	
6803	*AF*	Custom Audio I/O Chip B3 channel 2 produces pure tone.
6803	*00*	Custom Audio I/O Chip B3 channel 2 off.
600F	*00*	
600F	*03*	
6000	*55*	
6001	*AF*	Custom Audio I/O Chip C/D3 channel 1 produces pure tone.
6001	*00*	Custom Audio I/O Chip C/D3 channel 1 off.
6002	*55*	
6003	*AF*	Custom Audio I/O Chip C/D3 channel 2 produces pure tone.
6003	*00*	Custom Audio I/O Chip C/D3 channel 2 off.

F. Player and Option Switch Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{\text{W}}$: READ
3. For each address listed in Table 4, do the following:
   a. Set R/$\overline{\text{W}}$ MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/$\overline{\text{W}}$ MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address.

Table 4 Player and DIP Switch Inputs

ADDRESS	INPUT SWITCH	TEST RESULTS
7800	Right coin switch Left coin switch Self-test switch	Lower nybble (right digit) of DATA display changes when right or left coin, or self-test switches are activated. Upper nybble of DATA display is unstable.
8000	Player 1 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START	Upper nybble of DATA display changes when each input switch is activated.
8800	Player 2 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START	Upper nybble of DATA display changes when each input switch is activated.

G. Analog Vector-Generator

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. R/$\overline{\text{W}}$: WRITE
   c. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter address *2000* with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 5.
6. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
7. Repeat parts 4 through 6 for each address listed in Table 5 using the ADDRESS INCR button to advance the address by 1.

CAUTION

You may damage the circuitry of the X-Y display if you key in the $\overline{\text{VGGO}}$ signal without first checking all the addresses and data. Check the data by reading each address location using parts 8 though 11 below.

8. Set CAT Box switches as indicated:
   a. R/$\overline{\text{W}}$: READ
   b. R/$\overline{\text{W}}$ MODE: (OFF)
9. Enter address or press ADDRESS INCR.
10. Set R/$\overline{\text{W}}$ MODE to PULSE.
11. Check the data shown in the DATA display against that listed in Table 5. If the data is correct, proceed with part 12.
12. Set CAT Box switches as indicated:
    a. R/$\overline{\text{W}}$: WRITE
    b. R/$\overline{\text{W}}$ MODE: (OFF)

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13. Enter $\overline{\text{VGGO}}$ address *8840* .
14. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
15. Check that the screen shows a large plus sign. Failure of the horizontal or vertical circuits shows up as a single line drawn on the screen. *If the screen does not display a large plus sign, contact Atari Field Service.*

Table 5 Analog Vector-Generator Data

ADDRESS	DATA	ADDRESS	DATA
2000	*00*	*200C*	*00*
2001	*70*	*200D*	*21*
2002	*40*	*200E*	*80*
2003	*80*	*200F*	*1F*
2004	*77*	*2010*	*80*
2005	*64*	*2011*	*1F*
2006	*00*	*2012*	*00*
2007	*00*	*2013*	*01*
2008	*80*	*2014*	*00*
2009	*1F*	*2015*	*20*
200A	*00*	*2016*	*00*
200B	*00*	*2017*	*E0*

H. LED, Coin Counter, and Invert Outputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{\text{W}}$: WRITE
   d. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter address *8800* with the keyboard.

CAUTION

If you write ON data to activate a solenoid, *deactive the solenoid immediately* by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

4. For each DATA output listed in Table 5, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter the ON data listed for the output.
      - Set R/$\overline{\text{W}}$ MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter the OFF data listed for the output.
      - Set R/$\overline{\text{W}}$ MODE to STATIC and back to (OFF).

Table 6 LED and Coin Counter Outputs

ON DATA	OFF DATA	OUTPUT DEVICE
00	*10*	Player 1 LED
00	*20*	Player 2 LED
01	*00*	Right Coin Counter
02	*00*	Left Coin Counter
08	*00*	Coin Door Lockout
40	*00*	INVERT X*
80	*00*	INVERT Y**

*When INVERT X is activated, check for logic 1 on pin 16 of IC B10.

**When INVERT Y is activated, check for logic 1 on pin 16 of IC E10.

Troubleshooting with Signature Analysis

A. Signature Analysis Set-Up

1. Perform the CAT Box preliminary set-up.
2. Connect the three BNC-to-EZ clip cables supplied with CAT Box to the SIGNATURE ANALYSIS CONTROL START, STOP, and CLOCK jacks of the CAT Box.
3. Connect the three black EZ clips to a game PCB ground test point.
4. Connect the CAT Box DATA PROBE to the DATA jack on the CAT Box.
5. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. TESTER SELF-TEST: OFF
   c. PULSE MODE: LATCHED
   d. START: Negative-going edge trigger
   e. STOP: Negative-going edge trigger
   f. CLOCK: Negative-going edge trigger

B. Address Lines

1. Perform the signature analysis set-up.
2. Connect the START probe tip to pin 14 of IC R2.
3. Connect the STOP probe tip to pin 14 of IC R2.
4. Connect the CLOCK probe tip to Φ2 test point on the game PCB.
5. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT Box ADDRESS/SIGNATURE display should show *0000*. Now connect the DATA PROBE to a +5V test point; the ADDRESS/SIGNATURE display should show *0001*.
6. Probe the IC-pin listed in Table 7 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 7 Address Bus Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
C1-18	AB0	*UUUU*
C1-16	AB1	*5555*
C1-14	AB2	*CCCC*
C1-12	AB3	*7F7F*
C1-3	AB4	*5H21*
C1-5	AB5	*0AFA*
C1-7	AB6	*UPFH*
C1-9	AB7	*52F8*
B1-16	AB8	*HC89*
B1-14	AB9	*2H70*
B1-12	AB10	*HPP0*
B1-7	AB11	*1293*
B1-5	AB12	*HAP7*
R2-12	A13	*3C96*
R2-13	A14	*3827*
R2-14	A15	*755U*

C. Address Decoder

CAUTION

While testing decoders and ROMs, adding 270 pF capacitors to AB12, A13, A14, and A15 may be necessary to eliminate unstable signatures.

1. Perform parts 1 through 5 of the address bus signature procedure.
2. Probe the IC-pin listed in Table 8 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 8 Decoder Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
R2-1	$\overline{\text{RAM}}$	*3APF*
R2-2	$\overline{\text{I/O0}}$	*85H4*
R2-3	$\overline{\text{I/O1}}$	*131H*
R2-4	$\overline{\text{I/OS}}$	*96F9*
R2-5	$\overline{\text{EAROMRD}}$	*F042*
R2-6	$\overline{\text{SINP1}}$	*942F*
R2-7	$\overline{\text{SINP2}}$	*3PCF*
R2-9	$\overline{\text{IO}}$	*84AF*
R1-1	$\overline{\text{VMEM}}$	*U9U3*
R1-2	ROM	*FU4U*
R1-3	$\overline{\text{ROM0}}$	*H759*
R1-4	$\overline{\text{ROM1}}$	*A3UH*
R1-5	$\overline{\text{ROM2}}$	*AA6A*
R1-6	$\overline{\text{ROM3}}$	*A711*
R1-7	$\overline{\text{ROM4}}$	*54F5*
R1-9	$\overline{\text{ROM5}}$	*P255*

Watchdog Troubleshooting

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line.

RESET is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the RESET test point is grounded. A pulsing $\overline{\text{RESET}}$ line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing $\overline{\text{RESET}}$ signal indicates a problem exists somewhere within the microprocessor circuitry rather than within the analog vector-generator.

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Gravitar™ PCB Troubleshooting

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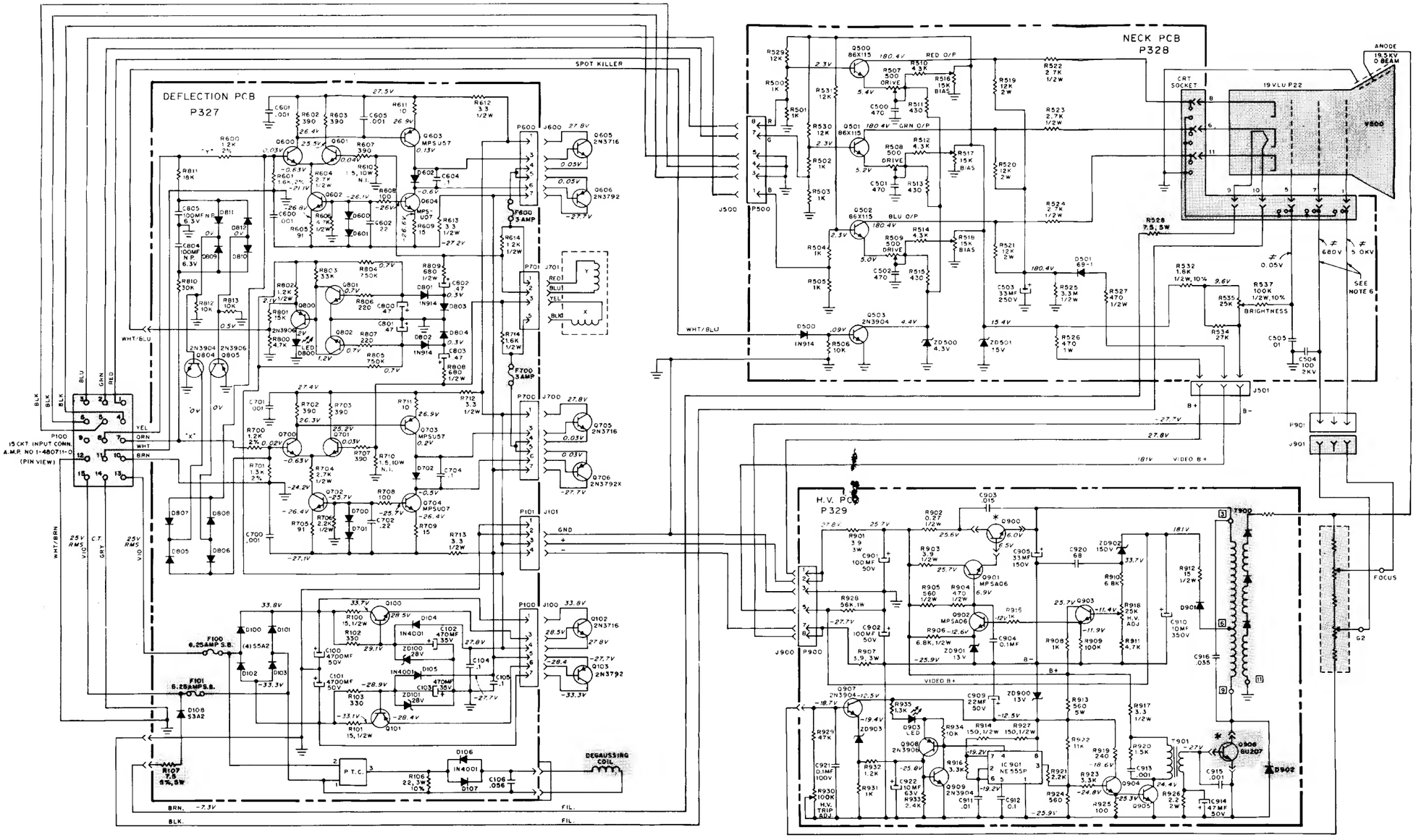

GENERAL NOTES

1. Resistance values in ohms, ¼ watt, ±5%, unless otherwise noted. K = 1,000, M = 1,000,000
2. Capacitance value of 1 or less is in microFarads, above 1 in picoFarads, unless otherwise noted.
3. * Q900 and Q906 are not in High-Voltage PCB.
4. All D.C. voltages are ±10% measured from point indicated to ground, using a high-impedance meter. Voltages are measured with no signal input and controls are in a normal operating position.
5. Circled numbers indicate location of waveform reading.
6. ZD100-101 uses (66X0040-007) zener diode in series with (340X2331-934) 330-ohm resistor in early production models.
7. Use a 1,000:1 probe when measuring G2 (screen) or focus voltage.

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Color X-Y Display Schematic Diagram

A Warner Communications Company

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